Super South Bridge

SiS 960

Preliminary

Rev. 0.5

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1. SiS960 OVERVIEW

The SiS960 is a highly integrated multifunctional component integrating conventional peripheral controllers and interfaces to obtain a high performance and cost effective design, as well as the advanced peripheral controllers and interfaces to make higher system design scaleable. The SiS960 conventional peripheral controllers and interfaces include:

- Support PCI Rev 2.1 Compliant PCI-To-LPC Bridge
- Integrated 8237 Compatible DMA Controllers
- Integrated 8259 Compatible Interrupt Controllers
- Integrated 8254 Compatible Timers
- Support ACPI Rev 1.0 And APM Rev.1.2 Advanced Power Management.
- Integrated Keyboard/PS2 Mouse Controller
- Real Time Clock with 256 Bytes CMOS SRAM and Multiple Alarm Function.
- Openhci USB Host Controller With Five USB Ports.
- Smbus Controller
- Integrated CPU Core Frequency Jumperless Setting Logic.

The SiS960 advanced peripheral controllers and interfaces include:

- Low Pin Count (LPC) Rev 1.0 Compliant Interface Support.
- AC' 97 Rev 2.1 Compliant Digital Controller and Interface Support.
- Game Port and MIDI Port Support.
- Two Device Bay Rev. 1.0 Compliant Controllers
- Integrated IEEE 802.3/802.3u Standard Compliant Fast Ethernet Controller and Physical Layer Transceiver

SiS960 is designed to integrate all peripheral controllers/accelerator/interfaces. SiS960 provides interface to Low Pin Count (LPC) operating at 33 MHz clock same as PCI clock on the host. This interface implementation is compliant with LPC Rev 1.0 Specification. The SiS960 AC' 97 interface implementation is based on Rev 2.1 of the AC' 97 Specification. The SiS960 AC' 97 interface supports up to two codecs, which can be selected as two audio codecs, or one audio codec plus one modem codec. In addition, the SiS960 digital audio controller provides 3D-hardware accelerator, on-chip sample rate convertor, and the advanced wavetable synthesizer. Moreover, SiS gives fully software support on both audio driver and V.90 modem driver. The SiS960 Device Bay controller/interface supports up to two USB devices (or 1394 device in the future) for easily adding and upgrading without opening the chassis. This interface implementation is compliant with Device Bay Rev. 1.0 Specification. The SiS960 Fast Ethernet controller and Physical Layer Transceiver supports fully duplex 10/100 Mbps operation and full OnNow features.

2. FEATURE

Low Pin Count Interface

- Forwards PCI I/O and Memory Cycles into LPC Bus
- Translates 8-/16-bit DMA Cycles into PCI Bus Cycles

Advanced PCI Audio & Modem

- Advanced Wavetable Synthesizer
  - 64-Voices Polyphony Wavetable Synthesizer Supports All Combinations of Stereo/Mono, 8-/16-bits, and Signed/Unsigned Samples
  - Per Channel Volume and Envelop Control, Pitch Shift, Left/Right Pan, Tremolo, and Vibrato
  - Global Effect Process for Reverb, Chorus and Echo
  - DirectMusic™ Support with Unlimited Downloadable Samples in System Memory
  - DLS-1-Compatible Downloadable Samples Support
- DirectSound™ 3D
  - 64-Voice DirectSound™ Channels
  - 32-Voice DirectSound™3D Accelerator With IID, IAD and Doppler Effects on 3D positional Audio buffer
  - DirectSound Accelerator for Volume, Pan and Pitch Shift Control on Streaming or Static Buffers
  - VirtualHRTF Interactive 3D Positional Audio Accelerator for DirectX™ 5/6
- Advanced Streaming Architecture
  - Microsoft WDM Streaming Architecture Compliant and Re-routable Endpoint Support
  - Three Stereo Capture Channels
  - AC97/98 Stereo Recording Channel Through AC-Link
- High Quality Audio and AC97/98 Support
  - CD Quality Audio With 90dB+ SNR Using External High Quality AC97/98 CODEC
  - AC97/98 Support With Full Duplex, Independent Sample Rate Converter for Audio Recording and Playback
  - On-chip Sample Rate Converter Ensures All Internal Operation at 48KHz
  - High Precision Internal 26-bit Digital Mixer with 20-bit Digital Audio Output
- Full Legacy Compatibility
  - SoundBlaster Pro/16
  - VirtualFM™ Enhances Audio Experience Through Real-time FM-to-Wavetable Conversion

  - MPU-401 Compatible UART for External or Internal Synthesis
  - VirtualGS provides General MIDI/GS Command Interpretation for Wavetable & Effect Synthesis
- Telephony & Modem
  - Full Duplex VirtualPhone Speaker Phone With Modem Capable AC97/98
  - HSP V.90 Modem
- Software Support
  - Complete DirectX driver suite(DirectSound3D, DirectSound, DirectMusic, DirectInput) for Windows 98/NT5.0
  - Configuration Installation and Diagnostics Under Real Mode DOS, Windows 98 DOS box
  - Windows 98/NT5.0 Configuration, Installation and Mixer Program
  - 1/2/4/8Mbytes General MIDI (GM) General Sound(GS) Compliant Sample Library
- Extras
  - Digital Enhanced Game Port Enables An Analog Joystick to Emulate Digital Joystick Performance using DirectInput driver. This eliminates up to 12% CPU overhead wasted on joystick polling
  - 2-to-6 speakers output with Optional VirtaulFX
  - VirtualAC3
  - DirectX timer for video/audio synchronization
  - I^2S and SPDIF Interface

Advanced Power Management For Desktop/Mobile Application

- Meets ACPI 1.0 Requirements
- Meets APM 1.2 Requirements
- ACPI Sleep States Include S1, S2, S3, S4, S5
- CPU Power States Include C0, C1, C2 C3
- Power Button with Override
- RTC Day-of-Month, Month-of-Year Alarm
- 24-bit Power Management Timer
- LED Blinking in S0,S1,S2 States
- System Power-Up Events Include: Power Button, Hot-Key, Keyboard Password, RTC Alarm, Modem Ring#, Device Bay, LAN, PME#
- Software Watchdog Timer
- Power Supply' 98 Support
- PCI Bus Power Management Interface Spec. 1.0
- Pentium II Sleep State

Integrated DMA Controller

- Two 8237A Compatible DMA Controllers
- 8/16- bit DMA Data Transfer

- Distributed DMA Support

Integrated Interrupt Controller

- Two 8259A Compatible Interrupt Controllers
- Level- or Edge-Triggered Programmable
- Serial IRQ
- Interrupt Sources Re-routable to Any IRQ Channel

Three 8254 Compatible Programmable 16-bit Counters

- System Timer Interrupt
- Generate Refresh Request
- Speaker Tone Output

Integrated Keyboard Controller

- Hardwired Logic Provides Instant Response
- Supports PS/2 Mouse
- Password Security And Password Power-Up
- System Sleep and Power-Up By Hot-Key
- KBC and PS2 Mouse Can Be Individually Disabled

Integrated Real Time Clock(RTC) with 256B CMOS SRAM

- Supports ACPI Day-of-Month and Month-of-Year Alarm
- 256 Bytes of CMOS SRAM
- Provides RTC year 2000 solution

Integrated CPU Core Frequency Jumperless Setting

Universal Serial Bus Host Controller

- OpenHCI Host Controller with Root Hub
- Five USB Ports Including two for Device Bay Connector
- Supports Legacy Devices
- Over Current Detection

Integrated Device Bay Controller

- Two ACPI-based Device Bay Controller
- Device Bay Events Wake Up

I^2C Bus/SMBUS

- Provides SMALERT# Pin

2Mbit Flash ROM Interface

Integrated Fast Ethernet controller and 10/100 megabit per second (Mbps) Physical Layer Transceivers for the PCI local bus

- 32-bit glueless PCI host interface
- Plug and Play compatible
- High-performance 32-bit PCI bus master architecture with integrated Direct Memory Access (DMA) Controller for low CPU and bus utilization

- Supports an unlimited PCI burst length
- Supports big endian and little endian byte alignments
- Supports PCI Device ID, Vendor ID/Subsystem ID, Subsystem Vendor ID programming through the EEPROM interface
- Implements optional PCI 3.3v auxiliary power source 3.3Vaux pin and optional PCI power management event (PME#) pin
- IEEE 802.3 and 802.3u standard compatible
- IEEE 802.3u Auto Negotiation and Parallel detection for automatic speed selection
- Full duplex and half duplex mode for both 10 and 100 Mbps.
- Fully compliant ANSI X3.263 TP-PMD physical sub-layer which includes adaptive equalization and Baseline Wander compensation.
- Automatic Jam and IEEE 802.3x Auto-Negotiation for flow control
- Single access to complete PHY register set
- Built-in waveform shaping requires no external filters
- Single 25Mhz clock for 10 and 100 Mbps operation.
- Power down of 10Base-T/100Base-TX sections when not in use
- Jabber control and auto-polarity correction for 10Base-T.
- User programmable LED function mapping
- Supports enhanced software, and automatic polling schemes to internal PHY status monitor
- Supports 10BASE-T, 100BASE-TX

Supports PC97, PC98, and Net PC requirements – Green PC compatible

- Supports Advanced Configuration and Power Interface Specification (ACPI) Revision 1.0
- Supports PCI Bus Power Management Interface Specification Version 1.0a
- Supports Network Device Class Power Management Specification Version 1.0a
- Supports PCI Hot-Plug Specification Revision 1.0
- Implements full OnNow features including pattern matching and link status wake-up with automatic internal PHY status polling
- Implements optional Magic Packet™ remote wake-up scheme
- Implements IEEE 802.3x compliant Flow Control

Additional features

- Internal 128-bit Multicast Hash Table address filter
- Serial EEPROM support
- Extensive programmable internal/external loopback capabilities

208 pins PQFP Package

2.1. FUNCTIONAL BLOCK DIAGRAM

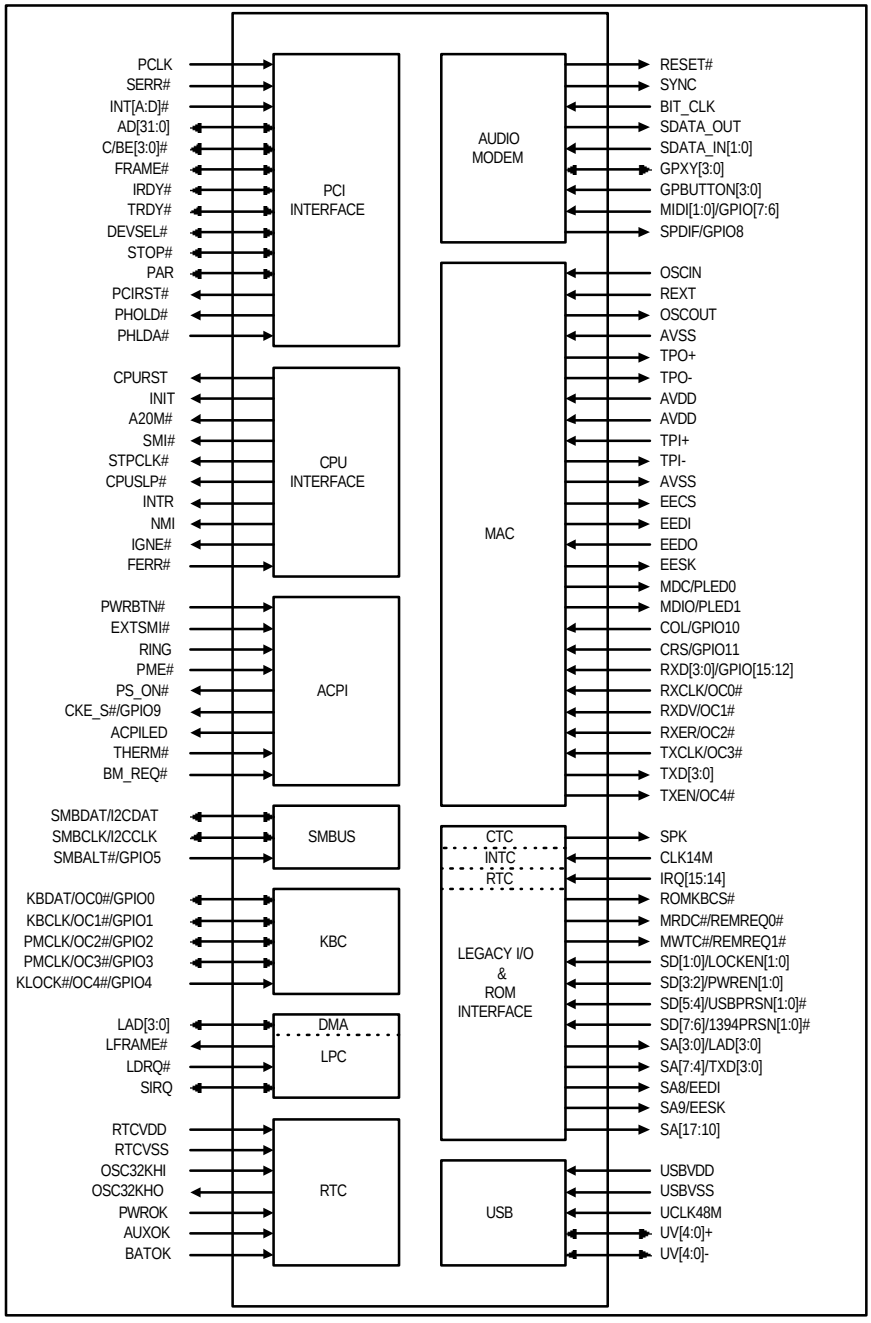


Figure 2.1-1Functional Block Diagram

3. PIN ASSIGNMENT

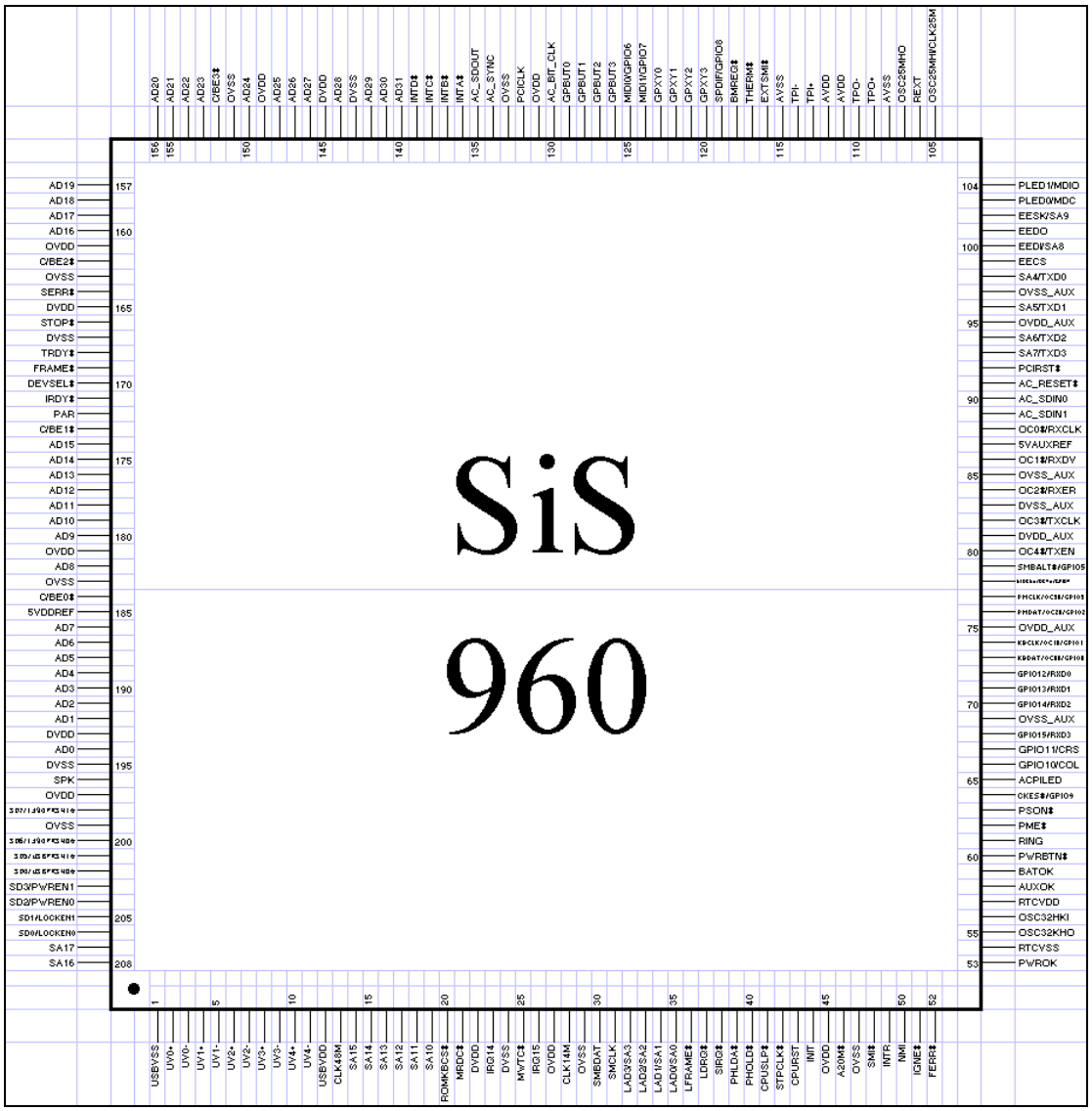


Figure 3-1 Pin Assignment

3.1. ALPHABETICAL PIN LIST

SIGNAL NAME	SiS960 BALL NO
USBVSS	1
UV0+	2
UV0-	3
UV1+	4
UV1-	5
UV2+	6
UV2-	7
UV3+	8
UV3-	9
UV4+	10
UV4-	11
USBVDD	12
CLK48M	13
SA15	14
SA14	15
SA13	16
SA12	17
SA11	18
SA10	19
ROMKBCS#	20
MRDC#	21
DVDD	22
IRQ14	23
DVSS	24
MWTC#	25
IRQ15	26
OVDD	27
CLK14M	28
OVSS	29

SIGNAL NAME	SiS960 BALL NO
SMBDAT	30
SMCLK	31
LAD3/SA3	32
LAD2/SA2	33
LAD1/SA1	34
LAD0/SA0	35
LFRAME#	36
LDRQ#	37
SIRQ#	38
PHLDA#	39
PHOLD#	40
CPUSLP#	41
STPCLK#	42
CPURST	43
INIT	44
OVDD	45
A20M#	46
OVSS	47
SMI#	48
INTR	49
NMI	50
IGNE#	51
FERR#	52
PWROK	53
RTCVSS	54
OSC32KHO	55
OSC32HKI	56
RTCVDD	57
AUXOK	58

SIGNAL NAME	SiS960 BALL NO
BATOK	59
PWRBTN#	60
RING	61
PME#	62
PSON#	63
CKES#/GPIO9	64
ACPILED	65
GPIO10/COL	66
GPIO11/CRS	67
GPIO15/RXD3	68
OVSS_AUX	69
GPIO14/RXD2	70
GPIO13/RXD1	71
GPIO12/RXD0	72
KBDAT/OC0#/GPIO0	73
KBCLK/OC1#/GPIO1	74
OVDD_AUX	75
PMDAT/OC2#/GPIO2	76
PMCLK/OC3#/GPIO3	77
KLOCK#/OC4#/GPIO4	78
SMBALT#/GPIO5	79
OC4#/TXEN	80
DVDD_AUX	81
OC3#/TXCLK	82
DVSS_AUX	83
OC2#/RXER	84
OVSS_AUX	85
OC1#/RXDV	86
5VAUXREF	87
OC0#/RXCLK	88

SIGNAL NAME	SiS960 BALL NO
AC_SDIN1	89
AC_SDIN0	90
AC_RESET#	91
PCIRST#	92
SA7/TXD3	93
SA6/TXD2	94
OVDD_AUX	95
SA5/TXD1	96
OVSS_AUX	97
SA4/TXD0	98
EECS	99
EEDI/SA8	100
EEDO	101
EESK/SA9	102
PLED0/MDC	103
PLED1/MDIO	104
OSC25MHI/CLK25M	105
REXT	106
OSC25MHO	107
AVSS	108
TPO+	109
TPO-	110
AVDD	111
AVDD	112
TPI+	113
TPI-	114
AVSS	115
EXTSMI#	116
THERM#	117
BMREQ#	118

SIGNAL NAME	SiS960 BALL NO
SPDIF/GPIO8	119
GPXY3	120
GPXY2	121
GPXY1	122
GPXY0	123
MIDI1/GPIO7	124
MIDI0/GPIO6	125
GPBUT3	126
GPBUT2	127
GPBUT1	128
GPBUT0	129
AC_BIT_CLK	130
OVDD	131
PCICLK	132
OVSS	133
AC_SYNC	134
AC_SDOUT	135
INTA#	136
INTB#	137
INTC#	138
INTD#	139
AD31	140
AD30	141
AD29	142
DVSS	143
AD28	144
DVDD	145
AD27	146
AD26	147
AD25	148

SIGNAL NAME	SiS960 BALL NO
OVDD	149
AD24	150
OVSS	151
C/BE3#	152
AD23	153
AD22	154
AD21	155
AD20	156
AD19	157
AD18	158
AD17	159
AD16	160
OVDD	161
C/BE2#	162
OVSS	163
SERR#	164
DVDD	165
STOP#	166
DVSS	167
TRDY#	168
FRAME#	169
DEVSEL#	170
IRDY#	171
PAR	172
C/BE1#	173
AD15	174
AD14	175
AD13	176
AD12	177
AD11	178

SIGNAL NAME	SiS960 BALL NO
AD10	179
AD9	180
OVDD	181
AD8	182
OVSS	183
C/BE0#	184
5VDDREF	185
AD7	186
AD6	187
AD5	188
AD4	189
AD3	190
AD2	191
AD1	192
DVDD	193

SIGNAL NAME	SiS960 BALL NO
AD0	194
DVSS	195
SPK	196
OVDD	197
SD7/1394PRSN1#	198
OVSS	199
SD6/1394PRSN0#	200
SD5/USBPRSN1#	201
SD4/USBPRSN0#	202
SD3/PWREN1	203
SD2/PWREN0	204
SD1/LOCKEN1	205
SD0/LOCKEN0	206
SA17	207
SA16	208

4. PIN DESCRIPTION

4.1. PCI BUS INTERFACE

SiS960 PIN NO.	NAME	TYPE ATTR	DESCRIPTION
	AD[31:0]	I/O	**PCI Address/Data Bus :** Comply with PCI specification 2.1
	C/BE[3:0]#	I/O	**PCI Bus Command and Byte Enables :** Comply with PCI specification 2.1
	DEVSEL#	I/O	**Device Select :** SiS960 will do positive decoding with medium timing to: - SiS960 configuration registers access - Built-in legacy embedded controller register access - BIOS ROM memory access - Interrupt acknowledge cycle In addition, SiS960 will do subtractive decoding to: - I/O address range 00000000h-0000FFFFh (low 64K bytes) - Full 32 bits memory address range
	FRAME#	I/O	**PCI FRAME# :** Comply with PCI specification 2.1
	INT[A:D]#	I	**PCI interrupt A,B,C,D :** The PCI interrupts will be connected to the inputs of the internal Interrupt controller through the rerouting logic associated with each PCI interrupt.
	IRDY#	I/O	**PCI IRDY# :** Comply with PCI specification 2.1
	PAR	I/O	**PCI Parity :** SiS960 always generates even-parity on PAR and ignores the parity driven by other PCI agents.
	PCICLK	I	**PCI Clock :** Comply with PCI specification 2.1
	PCIRST#	O	**PCI Bus Reset :** PCIRST# will be asserted during the period when PWROK is low, and will be kept on asserting until about 24ms after PWROK goes high.
	PHLDA#	I	**PCI Bus Hold Acknowledge :** The PCI system arbiter responds to the assertion of PHOLD# by driving PHLDA# low, indicating SiS960 can start its PCI master cycles.

	PHOLD#	O	**PCI Bus Hold Request :** PHOLD# is asserted to inform the PCI system arbiter located at north-bridge chipset that SiS960 is intending to become PCI bus master. SiS960 asserts PHOLD# on behalf of five local devices including distributed DMA master, USB master, MAC master, and AC'97 master.
	SERR#	I	**System Error :** When sampled active low, a non-maskable interrupt (NMI) can be generated to CPU if enabled.
	STOP#	I/O	**PCI STOP# :** Comply with PCI specification 2.1
	TRDY#	I/O	**PCI TRDY# :** Comply with PCI specification 2.1

4.2. CPU INTERFACE

SiS960 PIN NO.	NAME	TYPE ATTR	DESCRIPTION
	A20M#	OD	**Address 20 Mask :** When A20M# is asserted, the CPU A20 signal will be forced to '0'. **Speed Trap for PII :** This pin will be forced to voltage level according to the input value of SA14 or APC0h.5 during system reset period.
	CPURST	OD	**CPU Reset :** Active high signal to reset CPU.
	CPUSLP#	OD	**CPU Sleep :** SiS960 can optionally assert CPUSLP# to force the CPU into deep sleep mode when going to S2 state.
	FERR#	I	**Floating Point Error :** CPU will assert this signal upon a floating point error occurs.
	IGNE#	OD	**Ignore Numeric Error :** IGNE# is asserted to inform CPU to ignore a numeric error. **Speed Trap for PII :** This pin will be forced to voltage level according to the input value of SA13 or APC0h.4 during system reset period.

	INIT	OD	**Initialization :** INIT is used to re-start the CPU without flushing its internal caches and registers. In Pentium platform it is active low, while in Pentium II platform it is active high.
	INTR	OD	**Interrupt Request :** At high-level voltage on this signal indicates to the CPU that there is outstanding interrupt(s) need to be serviced. **Speed Trap for PII :** This pin will be forced to voltage level according to the input value of SA15 or APC0h.6 during system reset period.
	NMI	OD	**Non-Maskable Interrupt :** A rising edge on NMI will trigger a non-maskable interrupt to CPU. **Speed Trap for PII :** This pin will be forced to voltage level according to the input value of SA16 or APC0h.7 during system reset period.
	SMI#	OD	**System Management Interrupt :** SMI# will be asserted upon a pre-defined power management event occurs.
	STPCLK#	OD	**Stop Clock :** STPCLK# will be asserted to inhibit or throttle CPU activities upon a pre-defined power management event occurs.

4.3. POWER MANAGEMENT INTERFACE

SiS960 PIN NO.	NAME	TYPE ATTR	DESCRIPTION
	ACPILED	OD	**ACPILED :** ACPILED can be used to control the blinking of an LED at the frequency of 1 Hz to indicate the system is at power saving mode.
	BMREQ#	I	**Bus Mater Request:** This is a serial link from SiS north bridge chipset carrying the current AGP and PCI bus master information to SiS960 for power management purpose.

	CKE_S GPIO9	OD I/O/OD	**SDRAM Self-Refresh Enable :** When the system is in S3 mode (suspend to DRAM), the CKE_S is driven low to enable the self-refresh mode of SDRAM. **General Purpose Input/Output 9 :** Refer to GPIO description.
	EXTSMI#	I	**External SMI#:** EXTSMI# can be used to generate wakeup event, sleep event, or SCI/SMI#/GPEIRQ event to the ACPI-compatible power management unit.
	PCIPME#	I/O	**PCIPME# :** When the system is in power-down mode, an active low event on PCIPME# will cause the PSON# to go low and hence turn on the power supply. When the system is in suspend mode, an active PCIPME# event will cause the system wakeup and generate an SCI/SMI#/GPEIRQ.
	PSON#	OD	**ATX Power ON/OFF control:** PSON# is used to control the on/off state of the ATX power supply. When the ATX power supply is in the OFF state, an activated power-on event will force the power supply to ON state.
	PWRBTN#	I	**Power Button:** This signal is from the power button switch and will be monitored by the ACPI-compatible power management unit to switch the system between working and sleeping states.
	RING	I	**Ring Indication :** An active RING pulse and lasting for more than 4ms will cause a wakeup event for system to wake from S1~S5.
	THERM#	I	**Thermal Detect :** THERM# is connected to the internal ACPI-compatible power management unit as an indication of outstanding thermal event. An active THERM# event can be used to generate SCI/SMI#/GPEIRQ. If THERM# is activated for more than 2 second, a thermal override event will occur and the system will enter CPU thermal throttling mode automatically.

4.4. SMBUS INTERFACE

SiS960 PIN NO.	NAME	TYPE ATTR	DESCRIPTION

	SMBDAT I2CDAT	I/OD I/OD	**SMBus Data :** SMBus data input/output pin. **I2C Data :** I2C data input/output pin.
	SMBCLK I2CCLK	I/OD I/OD	**SMBus Clock :** SMBus clock input/output pin. **I2C Clock :** I2C clock input/output pin.
	SMBALT# I2CALT# GPIO5	I/OD I/OD I/O/OD	**SMBus Alert :** This pin is used for SMBus device to wake up the system from sleep state or to generate SCI/SMI# /GPEIRQ. **I2C Alert :** This pin is used for I2C device to wake up the system from sleep state or to generate SCI/SMI# /GPEIRQ. **General Purpose Input/Output 5 :** Refer to GPIO description.

4.5. KEYBOARD CONTROLLER INTERFACE

SiS960 PIN NO.	NAME	TYPE ATTR	DESCRIPTION
	KBDAT OC0# GPIO0	I/OD I I/O/OD	**Keyboard Dada :** When the internal keyboard controller is enabled, this pin is used as the keyboard data signal. **OC0# :** When this pin is configured as OC0#, it can detects USB Port 0 over current condition. **General Purpose Input/Output 0 :** Refer to GPIO description.
	KBCLK OC1# GPIO1	I/OD I I/O/OD	**Keyboard Clock :** When the internal keyboard controller is enabled, this pin is used as the keyboard clock signal. **OC1# :** When this pin is configured as OC1#, it can detects USB Port 1 over current condition. **General Purpose Input/Output 1 :** Refer to GPIO description.

	PMDAT OC2# GPIO2	I/OD I I/O/OD	**PS2 Mouse Data:** When the internal keyboard and PS2 mouse controllers are enabled, this pin is used as PS2 mouse data signal. **OC2# :** When this pin is configured as OC2#, it can detects USB Port 2 over current condition. **General Purpose Input/Output 2 :** Refer to GPIO description.
	PMCLK OC3# GPIO3	I/OD I I/O/OD	**PS2 Mouse Clock:** When the internal keyboard and PS2 mouse controllers are enabled, this pin is used as the PS2 mouse clock signal. **OC3# :** When this pin is configured as OC3#, it can detects USB Port 3 over current condition. **General Purpose Input/Output 3 :** Refer to GPIO description.
	KLOCK# OC4# GPIO4	I I I/O/OD	**Keyboard Lock:** When KLOCK# is tied low, the internal keyboard controller will not respond to any key-strikes. **OC4# :** When this pin is configured as OC4#, it can detects USB Port 4 over current condition. **General Purpose Input/Output 4 :** Refer to GPIO description.

4.6. LPC INTERFACE

SiS960 PIN NO.	NAME	TYPE ATTR	DESCRIPTION
	LAD[3:0] SA[3:0]	I/O O	**LPC Address/Data Bus :** LPC controller drives these four pins to transmit LPC command, address, and data to LPC device. **ROM Interface Address Bus :** In legacy ROM cycle, these four pin are used to drive address bus A[3:0] to access ROM.
	LDRQ#	I	**LPC DMA Request :** This pin is used by LPC device to request DMA cycle.
	LFRAME#	O	**LPC Frame :** This pin is used to notify LPC device that a start or a abort LPC cycle will occur.

	SIRQ	I/OD	**Serial IRQ :** This signal is used as the serial IRQ line signal.

4.7. RTC INTERFACE

SiS960 PIN NO.	NAME	TYPE ATTR	DESCRIPTION
	AUXOK	I	**Auxiliary Power OK :** This signal is supplied from the power source of resume well. It is also used to reset the logic in resume power well. If there is no auxiliary power source on the system, this pin should be tied together with PWROK. Note: No 5V tolerance for this pin. Please refer to SiS application circuit.
	BATOK	I	**Battery Power OK:** When the internal RTC is enabled, this signal is used to indicate that the power of RTC well is stable. It is also used to reset the logic in RTC well. If the internal RTC is disabled, this pin should be tied low. Note: No 5V tolerance for this pin. Please refer to SiS application circuit.
	OSC32KHI	I	**RTC 32.768 KHz Input :** When internal RTC is enabled, this pin provides the 32.768 KHz clock signal from external crystal or oscillator.
	OSC32KHO	O	**RTC 32.768 KHz Output :** When internal RTC is enabled, this pin should be connected the other end of the 32.768 KHz crystal or left unconnected if an oscillator is used.
	PWROK	I	**Main Power OK :** A high-level input to this signal indicates the power being supplied to the system is in stable operating state. During the period of PWROK being low, CPURST and PCIRST# will all be asserted until after PWROK goes to high for 24 ms. Note: No 5V tolerance for this pin. Please refer to SiS application circuit.

4.8. AC'97 AND GAME PORT INTERFACE

SiS960 PIN NO.	NAME	TYPE ATTR	DESCRIPTION

	AC_BITCLK	I	**AC'97 Bit Clock :** This signal is a 12.288MHz serial data clock, which is generated by primary Codec.
	AC_RESET#	O	**AC'97 Reset :** Hardware reset signal for external Codecs.
	AC_SDIN[1:0]	I	**AC'97 Serial Data input :** Serial data input from primary Codec and secondary Codec.
	AC_SDOUT	O	**AC'97 Serial Data output :** Serial data output to Codecs.
	AC_SYNC	O	**AC'97 Synchronization :** This is a 48KHz signal, which is used to synchronize the Codecs.
	GPXY[3:0]	I	**Game Port X/Y Coordinates :** These pins are the four axis coordinates for the game port.
	GPBTN[3:0]	I	**Game Port Buttons :** These pins are the four buttons for the game port.
	MIDIIN GPIO6	I I/O/OD	**MIDI Data Input :** This is the serial input pin for the internal MIDI port. **General Purpose Input/Output 6 :** Refer to GPIO description.
	MIDIOUT GPIO7	I I/O/OD	**MIDI Data Output :** This is the serial output pin for the internal MIDI port. **General Purpose Input/Output 7 :** Refer to GPIO description.
	SPDIF GPIO8	O I/O/OD	**S/PDIF Transmitter Output** **General Purpose Input/Output 8 :** Refer to GPIO description.

4.9. PHY AND SERIAL EEPROM INTERFACE

SiS960 PIN NO.	NAME	TYPE ATTR	DESCRIPTION
	EECS	O	**Serial EEPROM Chip Select :** This enables the EEPROM during loading of the Ethernet configuration data.

	EEDI SA8	O O	**Serial EEPROM Data Input :** During serial EEPROM access cycle, the SiS960 will use this pin to serially write OP codes, addresses and data into the serial EEPROM. **Legacy ROM Address Bus :** During legacy ROM access cycle, this pin acts as the address bus for ROM interface.
	EEDO	I	**Serial EEPROM Data Output :** During serial EEPROM access cycle, the SiS960 will read the contents of the EEPROM serially through this pin.
	EESK SA9	O O	**Serial EEPROM Clock :** This pin provides the clock for the serial EEPROM. **Legacy ROM Address Bus :** During legacy ROM access cycle, this pin acts as the address bus for ROM interface.
	OSC25MHI	I	**PHY 25MHz Clock Input :** This pin is supplied the 25MHz clock signal input from the external crystal or an oscillator.
	OSC25MHO	O	**PHY 25MHz Clock Output :** This pin should be connected the other end of the 25MHz crystal or left unconnected if an oscillator is used.
	PLED0# MDC	OD O	**Programmable LED0 Output :** The default function of PLED0# is to be a 10Mbps link detect output. This pin can also be programmed through the MI serial port to indicate other events or by user controlled. **Management Data Clock :** Clock signal with a maximum rate of 2.5MHz used to transfer management data for the external PMD on the MDIO pin.
	PLED1# MDIO	OD I/O	**Programmable LED1 Output :** The default function of PLED1# is to be a full duplex detect output. This pin can also be programmed through the MI serial port to indicate other events or by user controlled. **Management Data I/O :** Bi-directional signal used to transfer management information for the external PMD.
	REXT	I	**Transmit Current Set :** An external resistor connected between this pin and GND will set the output current level for the twisted pair outputs.

	TPIP	I	**Twisted Pair Receive Positive Input**
	TPIN	I	**Twisted Pair Receive Negative Input**
	TPOP	O	**Twisted Pair Transmit Positive Output**
	TPON	O	**Twisted Pair Transmit Negative Output**

4.10. USB INTERFACE

SiS960 PIN NO.	NAME	TYPE ATTR	DESCRIPTION
	CLK48M	I	**USB 48 MHz clock input :** This signal provides the fundamental clock for the USB Controller.
	OC0# RXCLK	I I	**USB Port 0 Over Current Detection :** OC0# is used to detect the over current condition of USB Port 0. **Receive Clock :** A continuous clock that is recovered from the incoming data. During 100Mb/s operation RXCLK is 25MHz and during 10Mb/s this is 2.5MHz.
	OC1# RXDV	I I	**USB Port 1 Over Current Detection :** OC1# is used to detect the over current condition of USB Port 1. **Receive Data Valid :** This indicates that the external physical unit is presenting recovered and decoded nibbles on RXD[3:0] and that RXCLK is synchronous to the recovered data. This signal will encompass the frame, starting with the SOF delimiter and excluding and EOF delimiter.
	OC2# RXER	I I	**USB Port 2 Over Current Detection :** OC2# is used to detect the over current condition of USB Port 2. **Receive Error :** This signal is asserted high synchronously by the external physical unit whenever it detects a media error and RXDV is asserted.
	OC3# TXCLK	I I	**USB Port 3 Over Current Detection :** OC3# is used to detect the over current condition of USB Port 3. **Transmit Clock :** A continuous clock that is source of the physical layer. During 100Mb/s operation, this is 25MHz. During 10Mb/s operation, this clock is 2.5MHz.

	OC4# TXEN	I O	**USB Port 4 Over Current Detection :** OC4# is used to detect the over current condition of USB Port 4. **Transmit Enable :** This signal is synchronous to TXCLK and provides precise framing for data carried on TXD[3:0]. It is asserted when TXD[3:0] contains valid data to be transmitted.
	USBP[4:0]P	I/O	**USB Port [4:0] Positive Input/Output**
	USBP[4:0]N	I/O	**USB Port [4:0] Negative Input/Output**

4.11. LEGACY I/O AND MISCELLANEOUS SIGNALS

SiS960 PIN NO.	NAME	TYPE ATTR	DESCRIPTION
	CLK14M	I	**14.318 MHz clock input :** This signal provides the fundamental clock for the 8254-compatible timer, and ACPI PM Timer.
	IRQ[15:14]	I	**Interrupt Request :** These are interrupt requests input to the internal 8259-compatible interrupt controller.
	MRDC# REMREQ0#	O I	**Memory Read Command :** MRDC# is asserted to indicate the addressed ROM device should drive its data onto the ROM data bus. **Removal Request 0 :** When device bay interface is enabled, this pin is used to indicate that the user wishes to remove the device form bay 0.
	MWTC# REMREQ1#	O I	**Memory Write Command :** MWTC# is asserted to strobe data into the addressed ROM device. **Removal Request 1 :** When device bay interface is enabled, this pin is used to indicate that the user wishes to remove the device form bay 1.
	ROMCS#	O	**Legacy ROM Chip Select :** ROMCS# will be asserted during legacy ROM access cycles.
	SA[17:10]	O	**Legacy ROM Address Bus :** These pins are used to drive the address of legacy ROM access cycle.

	SA[7:4] TXD[3:0]	O O	**Legacy ROM Address Bus :** These pins are used to drive the address of legacy ROM access cycle. **Transmit Data :** This is a group of 4 data signals that are driven synchronous to the TXCLK for transmission to the external physical unit.
	SD0 LOCKEN0	I/O O	**Legacy ROM Data Bit 0 :** This pin is used to send bit 0 of ROM data bus when a legacy ROM access cycle occurs. **Device Bay 0 Lock Enable :** This signal controls the software-controlled interlock mechanism of device bay 0.
	SD1 LOCKEN1	I/O O	**Legacy ROM Data Bit 1 :** This pin is used to send bit 1 of ROM data bus when a legacy ROM access cycle occurs. **Device Bay 1 Lock Enable :** This signal controls the software-controlled interlock mechanism of device bay 1.
	SD2 PWREN0	I/O O	**Legacy ROM Data Bit 2 :** This pin is used to send bit 2 of ROM data bus when a legacy ROM access cycle occurs. **Device Bay 0 Power Enable :** When this signal is asserted by device bay 0, it is used to enable the device that control VID0.
	SD3 PWREN1	I/O O	**Legacy ROM Data Bit 3 :** This pin is used to send bit 3 of ROM data bus when a legacy ROM access cycle occurs. **Device Bay 1 Power Enable :** When this signal is asserted by device bay 1, it is used to enable the device that control VID1.
	SD4 USBPRSN0#	I/O I	**Legacy ROM Data Bit 4 :** This pin is used to send bit 4 of ROM data bus when a legacy ROM access cycle occurs. **Present Signal for USB Device on Bay 0 :** When this pin is asserted, it means that a USB device is present on device bay 0.
	SD5 USBPRSN1#	I/O I	**Legacy ROM Data Bit 5 :** This pin is used to send bit 5 of ROM data bus when a legacy ROM access cycle occurs. **Present Signal for USB Device on Bay 1 :** When this pin is asserted, it means that a USB device is present on device bay 1.

	SD6 1394PRSN0#	I/O I	**Legacy ROM Data Bit 6 :** This pin is used to send bit 6 of ROM data bus when a legacy ROM access cycle occurs. **Present Signal for 1394 Device on Bay 0 :** When this pin is asserted, it means that a 1394 device is present on device bay 0.
	SD7 1394PRSN1#	I/O I	**Legacy ROM Data Bit 7 :** This pin is used to send bit 7 of ROM data bus when a legacy ROM access cycle occurs. **Present Signal for 1394 Device on Bay 1 :** When this pin is asserted, it means that a 1394 device is present on device bay 1.
	SPK	O	**Speaker output :** The SPK is connected to the system speaker.
	GPIO10 COL	I/O/OD I	**General Purpose Input/Output 10 :** Refer to GPIO description. **Collision Detected :** This signal is asserted high asynchronously by the external physical unit upon detection of a collision on the medium. It will remain asserted as long as the collision condition persists.
	GPIO11 CRS	I/O/OD I	**General Purpose Input/Output 11 :** Refer to GPIO description. **Carrier Sense :** This signal is asserted high asynchronously by the external physical unit upon detection of a non-idle medium.
	GPIO[15:12] RXD[3:0]	I/O/OD I	**General Purpose Input/Output [15:12] :** Refer to GPIO description. **Receive Data :** This is a group of 4 data signals aligned on nibble boundaries that are driven synchronous to the RXCLK by the external physical unit.

4.12. POWER PINS

SiS960 PIN NO.	NAME	TYPE ATTR	DESCRIPTION
	VDD[9:0]	PWR	**+3.3V DC Main Power Supply :** This is the power source for the core well and will be shut off in S3/S4/S5, or G3 states.
	AUXVDD[2:0]	PWR	**+3.3V DC Auxiliary Power Supply :** This is the power source for the resume well and won't be shut off unless a power failure event occurs.

	RTCVDD	PWR	**+3.3V DC Battery Power Supply :** This is the power source for the RTC well and won't be shut off unless the battery is removed or exhausted.
	USBVDD	PWR	**+3.3V DC Power Supply for USB Circuit :** This is the power source for the USB circuit. USBVDD can be applied from core or resume well.
	PHYVDD[1:0]	PWR	**+3.3V DC Power Supply for PHY Circuit :** This is the power source for the PHY circuit and must be applied from resume well.
	5VDDREF	PWR	**+5V Main Power Reference Voltage :** This reference voltage provides +5V tolerance for the core well circuit.
	5AUXREF	PWR	**+5V Auxiliary Power Reference Voltage :** This reference voltage provides +5V tolerance for the resume well circuit.
	VSS[19:0]	PWR	**Grounds**

5. FUNCTION DESCRIPTION

6. HARDWARE TRAP

The ROMCS#, and SA[17:10] pins can be used to configure SiS960 during system boot-up. The SiS960's operating mode will be determined by the voltage-level being applied to these pins when the PWRGD signal is going from low to high, known as Hardware Trap. A logic "1" will be recognized and trapped into internal control circuitry if an external pull-up resistor is connected to the trap pin, while a logic "0" will be trapped if a pull-down resistor is connected.

SiS960 PIN NO.	NAME	DESCRIPTION
	ROMCS#	**Enable/Disable System Auto-Reset Function** If the auto-reset function is enabled, PCIRST# will be asserted every 5~6 seconds unless the software disable the function by writing a zero to ACPI56h.6. Pull-up : Enable Pull-down : Disable
	SA17	**Enable/Disable Legacy ROM Interface** If the legacy ROM Interface is enabled, the ROM access cycle will be forwarded to legacy ROM interface. If it is disabled, the ROM access cycle will be forward to LPC interface. Pull-up : Enable Pull-down : Disable
	SA16	**PII CPU Speed Trap for NMI** The voltage level on this pin will be forwarded to NMI during CPURST period and till 7 PCICLK after CPURST is deasserted. It is used to determine PII CPU Core/Bus frequency ratio. In P5 platform, this pin should be pulled low.
	SA15	**PII CPU Speed Trap for INTR** The voltage level on this pin will be forwarded to INTR during CPURST period and till 7 PCICLK after CPURST is deasserted. It is used to determine PII CPU Core/Bus frequency ratio. In P5 platform, this pin should be pulled low.
	SA14	**PII CPU Speed Trap for A20M#** The voltage level on this pin will be forwarded to A20M# during CPURST period and till 7 PCICLK after CPURST is deasserted. It is used to determine PII CPU Core/Bus frequency ratio. In P5 platform, this pin should be pulled high.
	SA13	**PII CPU Speed Trap for IGNE#** The voltage level on this pin will be forwarded to IGNE# during CPURST period and till 7 PCICLK after CPURST is deasserted. It is used to determine PII CPU Core/Bus frequency ratio. In P5 platform, this pin should be pull high.

SiS960 PIN NO.	NAME	DESCRIPTION
	SA12	**Enable/Disable Internal PLL** If the internal PLL is enable, this will improve the timing of PCICLK. Pull-up : Enable Pull-down : Disable
	SA11	**Pentium/Pentium II Platform Select** Pull-up : Select Pentium platform Pull-down : Select Pentium II platform
	SA10	**Enable/Disable NAND Tree Test** Pull-up : Disable NAND tree test Pull-down : Enable NAND tree test

7. REGISTER SUMMARY

7.1. LPC BRIDGE CONFIGURATION REGISTERS

ADDRESS	ACCESS	REGISTER NAME
00-01h	RO	Vendor ID
02-03h	RO	Device ID
04-05h	RO	Command Register
06-07h	RO	Status register
08h	RO	Revision ID
09-0Bh	RO	Class Code
0Ch	RO	Cache Line Size
0Dh	RO	Master Latency Timer
0Eh	RO	Header Type
0Fh	RO	Built-in Self Test
10-3Ch	RO	- Reserved
40h	R/W	BIOS Control Register
41-44h	R/W	PCI INTA#/B#/C#/D# Remapping Register
45h	R/W	Flash ROM Control Register
46h	R/W	INIT Enable Register
47h	R/W	Keyboard Controller Register
48h	R/W	RTC Control Register
49h	R/W	Individual Distributed DMA Channel Enable Register
4A-4Bh	R/W	Distributed DMA Master Configuration Register
4C-4Fh	RO	Shadow Register of ICW1 to ICW4 of the INT1
50-53h	RO	Shadow Register of ICW1 to ICW4 of the INT2
54-55h	RO	Shadow Register of OCW 2&3 of INT1
56-57h	RO	Shadow Register of OCW 2&3 of the INT2
58h-5Fh	RO	CTC Shadow Registers 1 to 8
60h	RO	Shadow Register for ISA Port 70
61h	R/W	IDEIRQ Remapping Register
62h	R/W	USBIRQ Remapping Register
63h	R/W	GPEIRQ Remapping Register
64h	R/W	Priority Timer
65h	R/W	PHOLD# Timer
66h	R/W	Fixed Priority Selection
67h	R/W	Clear SIRQ1 and SIRQ12
68h	R/W	USB & ACPI/SCI IRQ Remapping Register
69h	R/W	Audio & MAC IRQ Remapping Register
6Ah	R/W	ACPI/SCI IRQ Remapping Register

6Bh	R/W	Device Bay IRQ Remapping Register
6Ch	R/W	SMBUS IRQ Remapping Register
6Dh	R/W	Software Watchdog IRQ Remapping Register
6E-6Fh	R/W	Software-Controlled Interrupt Requests
70h	R/W	Serial Interrupt Control Register
71-73h	R/W	Serial Interrupt Enable Register
74-75h	R/W	ACPI Base Address Register

7.2. LEGACY ISA REGISTERS

7.2.1. DMA REGISTERS

(These registers can be accessed from PCI bus and ISA bus)

ADDRESS	ACCESS	REGISTER NAME
0000h	R/W	DMA1 CH0 Base and Current Address Register
0001h	R/W	DMA1 CH0 Base and Current Count Register
0002h	R/W	DMA1 CH1 Base and Current Address Register
0003h	R/W	DMA1 CH1 Base and Current Count Register
0004h	R/W	DMA1 CH2 Base and Current Address Register
0005h	R/W	DMA1 CH2 Base and Current Count Register
0006h	R/W	DMA1 CH3 Base and Current Address Register
0007h	R/W	DMA1 CH3 Base and Current Count Register
0008h	R/W	DMA1 Status(r) Command(w) Register
0009h	R/W	DMA1 Request Register
000Ah	R/W	DMA1 Command(r) Write Single Mask Bit (w) Register
000Bh	R/W	DMA1 Mode DMA Register
000Ch	WO	DMA1 Clear Byte Pointer
000Dh	WO	DMA1 Master Clear
000Eh	WO	DMA1 Clear Mask Register
000Fh	R/W	DMA1 Write All Mask Bits(w) Mask Status(r) Register
00C0h	R/W	DMA2 CH0 Base and Current Address Register
00C2h	R/W	DMA2 CH0 Base and Current Count Register
00C4h	R/W	DMA2 CH1 Base and Current Address Register
00C6h	R/W	DMA2 CH1 Base and Current Count Register
00C8h	R/W	DMA2 CH2 Base and Current Address Register
00CAh	R/W	DMA2 CH2 Base and Current Count Register
00CCh	R/W	DMA2 CH3 Base and Current Address Register
00CEh	R/W	DMA2 CH3 Base and Current Count Register
00D0h	R/W	DMA2 Status(r) Command(w) Register
00D2h	R/W	DMA2 Request Register
00D4h	R/W	DMA2 Command(r) Write Single Mask Bit(w) Register

00D6h	R/W	DMA2 Mode Register
00D8h	WO	DMA2 Clear Byte Pointer
00DAh	WO	DMA2 Master Clear
00DCh	WO	DMA2 Clear Mask Register
00DEh	R/W	DMA2 Write All Mask Bits(w) Mask Status Register(r)

(These registers can be accessed from PCI bus or ISA bus)

ADDRESS	ACCESS	REGISTER NAME
0080h	R/W	Reserved
0081h	R/W	DMA Channel 2 Low Page Register
0082h	R/W	DMA Channel 3 Low Page Register
0083h	R/W	DMA Channel 1 Low Page Register
0084h	R/W	Reserved
0085h	R/W	Reserved
0086h	R/W	Reserved
0087h	R/W	DMA Channel 0 Low Page Register
0088h	R/W	Reserved
0089h	R/W	DMA Channel 6 Low Page Register
008Ah	R/W	DMA Channel 7 Low Page Register
008Bh	R/W	DMA Channel 5 Low Page Register
008Ch	R/W	Reserved
008Dh	R/W	Reserved
008Eh	R/W	Reserved
008Fh	R/W	Reserved

(These registers can be accessed from PCI bus or ISA bus)

ADDRESS	ACCESS	REGISTER NAME
00480h	R/W	Reserved
00481h	R/W	DMA Channel 2 High Page Register
00482h	R/W	DMA Channel 3 High Page Register
00483h	R/W	DMA Channel 1 High Page Register
00484h	R/W	Reserved
00485h	R/W	Reserved
00486h	R/W	Reserved
00487h	R/W	DMA Channel 0 High Page Register
00488h	R/W	Reserved
00489h	R/W	DMA Channel 6 High Page Register
0048Ah	R/W	DMA Channel 7 High Page Register
0048Bh	R/W	DMA Channel 5 High Page Register
0048Ch	R/W	Reserved

0048Dh	R/W	Reserved
0048Eh	R/W	Reserved
0048Fh	R/W	Reserved

7.2.2. INTERRUPT CONTROLLER REGISTERS

(These registers can be accessed from PCI bus or ISA bus.)

ADDRESS	ACCESS	REGISTER NAME
0020h	R/W	INT 1 Base Address Register
0021h	R/W	INT 1 Mask Register
00A0h	R/W	INT 2 Base Address Register
00A1h	R/W	INT 2 Mask Register

7.2.3. TIMER REGISTERS

(These registers can be accessed from PCI bus or ISA bus.)

ADDRESS	ACCESS	REGISTER NAME
0040h	R/W	Interval Timer 1 - Counter 0
0041h	R/W	Interval Timer 1 - Counter 1
0042h	R/W	Interval Timer 1 - Counter 2
0043h	WO	Interval Timer 1 - Control Word Register

7.2.4. OTHER REGISTERS

(These registers can be accessed from PCI bus or ISA bus.)

ADDRESS	ACCESS	REGISTER NAME
0061h	R/W	NMI Status Register
0070h	WO	CMOS RAM Address and NMI Mask Register
0092h	R/W	INIT and A20 Register
00F0h	WO	Coprocessor Error Register
04D0h	R/W	IRQ Edge/Level Control Register 1
04D1h	R/W	IRQ Edge/Level Control Register 2

7.3. ACPI CONFIGURATION REGISTERS

OFFSET	BYTE LENGTH	ACCESS	NAME	ABBREVIATE
00	2	R/WC	Power Management Status	PM1_STS
02	2	R/W	Power Management Enable	PM1_EN
04	2	R/W	Power Management Control	PM1_CNT
06	2	RO	Reserved	
08	4	RO	Power Management Timer	PM_TMR
0C	4	RO	Reserved	
10	4	R/W	Processor Control	P_CNT

14	1	RO	Processor Power State Level 2	P_LVL2
15	1	RO	Processor Power State Level 3	P_LVL3
16	4	RO	Reserved	
1A	2	R/W	Fix Feature Control	FIX_CNT
1C	2	WO	PM1_STS Write Port	PM1_PORT
1E	2	RO	Reserved	
20	2	R/WC	General Purpose Event 0 Status	GPE0_STS
22	2	R/W	General Purpose Event 0 Enable	GPE0_EN
24	4	R/W	GPE0 Interrupt Routing	GPE0_ROUT
28	2	R/W	GPE0 Trigger Mode Select	GPE0_TRG
2A	2	R/W	General Purpose Event Control	GPE_CNT
2C	2	WO	GPE0_STS Write Port	GPE0_PORT
2E	2	RO	Reserved	
30	2	R/WC	General Purpose Event 1 Status	GPE1_STS
32	2	R/W	General Purpose Event 1 Enable	GPE1_EN
34	4	R/W	GPE1 Interrupt Routing	GPE1_ROUT
38	2	R/W	GPE1 Trigger Mode Select	GPE1_TRG
3A	2	R/W	GPE1 Pin Level	GPE1_LVL
3C	2	R/W	GPE1 I/O Mode Select	GPE1_IO
3E	2	R/W	GPE1 Input Polarity Select	GPE1_POL
40	2	R/WC	Legacy Event Status	LEG_STS
42	2	R/W	Legacy Event Enable	LEG_EN
44	2	R/W	Device Activity Status	DEVACT_STS
46	2	RO	Reserved	
48	1	R/W	SMI# Command Port	SMICMD_PORT
49	1	R/W	Mail Box	MAIL_BOX
4A	1	R/W	Software Watchdog Timer Control	SFTMR_CNT
4B	1	R/W	SFTMR Initial Value	SF_TMR
4C	4	RO	High Resolution Timer Value	HR_TMR
50	2	R/W	PIO Port Trap 0 Address	IOTRAP0_PORT
52	2	R/W	PIO Port Trap 1 Address	IOTRAP1_PORT
54	1	R/W	PIO Port Trap 0 Mask	IOTRAP0_MASK
55	1	R/W	PIO Port Trap 1 Mask	IOTRAP1_MASK
56	2	R/W	Legacy Event Control	LEG_CNT
58	2	WO	LEG_STS Write Port	LEG_PORT
5A	2	R/W	IRQ/NMI Wake Control	IOQWAK_CNT
5C	2	RO	I/O Address Track for SMI#	ADDR_TRACK
5E	1	RO	I/O C/BE# Track for SMI	CBE_TRACK
5F	1	R/W	I2C Bus Control	I2C_CNT
60	2	RO	System Wakeup From S5 Status	S5WAK_STS

62	2	R/W	System Wakeup From S5 Control	S5WAK_CNT

7.4. SMBUS CONTROL REGISTERS

OFFSET	BYTE LENGTH	ACCESS	NAME	ABBREVIATE
80	1	R/WC	SMBUS Status	SMB_STS
81	1	R/W	SMBUS Enable	SMB_EN
82	1	R/W	SMBUS Control	SMB_CNT
83	1	R/W	SMBUS Host Control	SMBHOST_CNT
84	1	R/W	SMBUS Address	SMB_ADDR
85	1	R/W	SMBUS Command	SMB_CMD
86	1	RO	SMBUS Processed Byte Count	SMB_PCOUNT
87	1	R/W	SMBUS Byte Count	SMB_COUNT
88	8	R/W	SMBUS Byte0~7	SMB_BYTE0~7
90	1	R/W	SMBUS Device Address	SMBDEV_ADDR
91	1	R/W	SMBUS Device Byte 0	SMB_DB0
92	1	R/W	SMBUS Device Byte 1	SMB_DB1
93	1	R/W	SMBUS Host Slave Alias Address	SMB_SAA

7.5. SMBUS CONTROL REGISTERS

OFFSET	BYTE LENGTH	ACCESS	NAME	ABBREVIATE
A0	2	RO	DBC Vender ID	DBC_VID
A2	2	RO	Reserved	
A4	1	RO	DBC Revision ID	DBC_RID
A5	7	RO	Reserved	
AC	4	RO	DBC Capabilities Register	DBCCR
B0	4	R/WC	Device Bay 0 Status	BSTR0
B4	4	R/W	Device Bay 0 Control and Enable	BCER0
B8	4	R/WC	Device Bay 1 Status	BSTR1
BC	4	R/W	Device Bay 1 Control and Enable	BCER1

7.6. MAC AND PHY REGISTERS

7.6.1. MAC CONFIGURATION SPACE (FUNCTION 1)

CONFIGURATION. OFFSET	ACCESS	MNEMONIC REGISTER
00-01h	RO	Vendor ID
02-03h	RO	Device ID
04-05h	R/W	Command Register
06-07h	R/W	Status Register

08h	RO	Revision ID
09-0Bh	RO	Class Code
0Ch	RO	Cache Line Size
0Dh	R/W	Master Latency Timer
0Eh	RO	Header Type
0Fh	RO	Built-in Self Test
10-13h	R/W	Configuration IO Base Address Register
14-17h	R/W	Configuration Memory Address Register
18-28h	RO	RESERVED (reads return zero)
2C-2Fh	R/W	Configuration Subsystem Identification Register
30-33h	R/W	Configuration Expansion ROM Base Address Register
34-37h	R/W	Configuration Capabilities Pointer Register
38-3Bh	RO	RESERVED (reads return zero).
3C-3Fh	R/W	Configuration Interrupt Select Register
40-43h	R/W	Configuration Power Management Capabilities Register
44-47h	R/W	Configuration Power Management Control and Status Register
48-FFh	RO	RESERVED (reads return zero)

7.6.2. MAC OPERATIONAL REGISTERS

CONFIGURATION. OFFSET	ACCESS	MNEMONIC REGISTER
00-03h	R/W	Command Register
04-07h	R/W	Configuration Register
08-0Bh	R/W	EEPROM Access Register
0C-0Fh	R/W	PCI Test Control Register
10-13h	R/W	Interrupt Status Register
14-17h	R/W	Interrupt Mask Register
18-1Bh	R/W	Interrupt Enable Register
1C-1Fh	R/W	Enhanced PHY Access Register
20-23h	R/W	Transmit Descriptor Pointer Register
24-27h	R/W	Transmit Configuration Register
28-2Fh	R/W	RESERVED
30-33h	R/W	Receive Descriptor Pointer Register
34-37h	R/W	Receive Configuration Register
38-3Bh	R/W	Flow Control Register
3C-47h	RO	RESERVED
48-4Bh	R/W	Receive Filter Control Register
4C-4Fh	R/W	Receive Filter Data Register

50-AFh	RO	RESERVED
B0-B3h	R/W	Power Management Control Register
B4-B7h	R/W	Power Management Wake-up Event Register
B8-BBh	R/W	RESERVED
BC-BFh	R/W	Wake-up Sample Frame CRC Register
C0-EFh	R/W	Wake-up Sample Frame Mask Registers
F0-FFh	R/W	RESERVED

7.6.3. PHY CONFIGURATION REGISTERS

CONFIGURATION. OFFSET	ACCESS	MNEMONIC REGISTER
00h	R/W	MI Register 0 Control Register
01h	R/W	MI Register 1 Status Register
02h	R/W	MI Register 2 PHY ID#1
03h	R/W	MI Register 3 PHY ID#2
04h	R/W	MI Register 4 Auto Negotiation Advertisement
05h	R/W	MI Register 5 Auto Negotiation Remote End Capability
10h	R/W	MI Register 16 Configuration 1
11h	R/W	MI Register 17 Configuration 2
12h	R/W	MI Register 18 Status Output
13h	R/W	MI Register 19 Mask
14h	R/W	MI Register 20 Reserved

7.7. USB OHCI HOST CONTROLLER CONFIGURATION SPACE

7.7.1. USB CONFIGURATION SPACE (FUNCTION 2)

CONFIGURATION. OFFSET	ACCESS	MNEMONIC REGISTER
00-01h	RO	VID Vendor ID
02-03h	RO	DID Device ID
04-05h	R/W	CMD Command Register
06-07h	R/W	STS Status register
08h	RO	RID Revision ID
09-0Bh	RO	CD Class Code
0Ch	RO	CL Cache Line Size
0Dh	R/W	MLT Master Latency Timer
0Eh	RO	HT Header Type
0Fh	RO	BIST Built-in Self Test
10-13h	R/W	Base address
13-3Bh	RO	- Reserved

3Ch	R/W	INTL Interrupt line
3Dh	RO	INTP Interrupt pin
3Eh	RO	MINGNT Min Gnt
3Fh	RO	MAXLAT Max Latency

7.7.2. HOST CONTROLLER OPERATIONAL REGISTERS

OFFSET	3100
0	HcRevision
4	HcControl
8	HcCommandStatus
C	HcInterruptStatus
10	HcInterruptEnable
14	HcInterruptDisable
18	HcHCCA
1C	HcPeriodCurrentED
20	HcControlHeadED
24	HcControlCurrentED
28	HcBulkHeadED
2C	HcBulkCurrentED
30	HcDoneHead
34	HcFmInterval
38	HcFmRemaining
3C	HcFmNumber
40	HcPeriodicStart
44	HcLSThreshold
48	HcRhDescriptorA
4C	HcRhDescriptorB
50	HcRhStatus
54	HcRhPortStatus[1]
58	HcRhPortStatus[2]
5C	HcRhPortStatus[3]
60	HcRhPortStatus[4]
64	HcRhPortStatus[5]
100	HceControl
104	HceInput
108	HceOutput
10C	HceStatus

7.7.3. AUDIO CONFIGURATION SPACE (FUNCTION 3)

CONFIGURATION. OFFSET	ACCESS	MNEMONIC REGISTER
00-01h	R/W	Vendor ID
02-03h	R/W	Device ID
04-05	R/W	Command
06-07h	R/W	Status
08h	RO	Revision ID
0A-0Bh	RO	Class Code
0Ch	R/W	Cache Line Size
0Dh	R/W	Latency Timer
0Eh	R/W	Header Type
0Fh	R/W	BIST
10-13h	R/W	Audio IO Base Address
14-17h	R/W	Audio Memory Base Address
18-28h	RO	RSVD
2C-2Dh	R/W	Subsystem Vendor ID
2E-2Fh	R/W	Subsystem ID
30-33h	R/W	RSVD
34h	RO	PCIPM Capability List Pointer
35-37h	RO	RSVD
38h	RO	RSVD
3Ch	R/W	Interrupt Line
3Dh	R/W	Interrupt Pin
3Eh	R/W	MIN_GNT
3Fh	R/W	MAX_LAT
40-43h	R/W	DDMA Slave Configuration
44h	R/W	Legacy audio/ power management configuration LEGACY_IOBASE
45h	R/W	legacy DMA decoding
46h	R/W	Power Management Configuration
47h	R/W	Inactivity Timer Expiration Control
48h	R/W	INT Acknowledge Snoop
49h	R/W	INT_VEC
4A-4Bh	RO	RSVD
4C-DBh	RO	RSVD
DCh	R/W	PM_Cap_ID
DEh	R/W	PM_Next_Ptr
DFh	R/W	PMC
E0-E1h	R/W	PCI Configuration Address PMCSR
E2h	R/W	PCI Configuration Address PMCSR_BSE

E3h	R/W	PCI Configuration Address Power Value Data

7.7.4. AUDIO OPERATIONAL REGISTERS

CONFIGURATION. OFFSET	ACCESS	MNEMONIC REGISTER
00h	R/W	Legacy DMA Playback Buffer Base Register Port 1
01h	R/W	Legacy DMA Playback Buffer Base Register Port 2
02h	R/W	Legacy DMA Playback Buffer Base Register Port 3
03h	R/W	Legacy DMA Playback Buffer Base Register Port4
04h	R/W	Legacy DMA Playback Byte Count Register 1
05h	R/W	Legacy DMA Playback Byte Count Register 2
06h	R/W	Legacy DMA Playback Byte Count Register 3
07h	R/W	Legacy DMA Playback Misc. Register
08h	RO	Legacy DMA Controller Command / Status Register
0Ah	WO	Legacy DMA Single Channel Mask Port
0Bh	R/W	Legacy DMA Channel Operation Mode Register
0Ch	WO	Legacy DMA Controller First_Last Flag Clear Port
0Dh	WO	Legacy DMA Controller Master Clear Port
0Eh	WO	Legacy DMA Controller Clear Mask Port
0Fh	WO	Legacy DMA Controller Multi-Channel Mask Register
10h	R/W	Legacy FmMusic Bank 0 Register Index / Legacy FmMusic Status
11h	R/W	Legacy FmMusic Bank 0 Register Data Port
12h	R/W	Legacy FmMusic Bank 1 Register Index
13h	R/W	Legacy FmMusic Bank 1 Register Data Port
14h	R/W	Legacy Sound Blaster Mixer Register Index
15h	R/W	Legacy Sound Blaster Mixer Register Data Port
16-18h	WO	Legacy Sound Blaster ESP Reset Port
1A-1Bh	RO	Legacy Sound Blaster ESP Data Port
1C-1Dh	R/W	Legacy Sound Blaster Command / Status Port
1Eh	RO	Legacy Sound Blaster ESP Data Ready / IRQ Acknowledge Port 1
1Fh	RO	Legacy Sound Blaster ESP Data Ready / IRQ Acknowledge Port 2
20h	R/W	Legacy MPU-401 Data Port / IRQ Acknowledge Port
21h	R/W	Legacy MPU-401 Command / Status Port
22h	R/W	MPU-401 Operation Control / Status Register
23h	R/W	MPU-401 MIDI-IN FIFO Access Port
30h	R/W	Gameport Control Register

31h	R/W	Legacy Gameport I/O Register
34h	RO	Enhanced Gameport Position Register 1
38h	RO	Enhanced Gameport Position Register 2
40h	R/W	AC-97 Mixer Write Register
44h	R/W	AC-97 Mixer Read Register
48h	R/W	Serial INTF Control Register
4Ch	R/W	AC97 General Purpose IO Register
50h	RO	TSAudio Status Register
54h	RO	Legacy Sound Blaster Frequency Read Back Register
56h	RO	Legacy Sound Blaster Time Constant Read Back Register
58h	R/W	TSAudio Scratch Register
5Ch	RO	TSAudio Version Control Register
5Eh	R/W	SB ESP Version High Byte Control Register
5Fh	R/W	SB ESP Version Low Byte Control Register
60h	RO	OPL3 Emulation Channel Keyon/off Trace Register
70h	R/W	S/PDIF Channel Status Register
74h	R/W	New Sub-system ID & Sub-vendor ID
78h	R/W	EEPROM interface control register
7Ch	R/W	General purpose IO Register
80h	R/W	START command and status register for Bank A
84h	R/W	Channel STOP command and status register for Bank A
88h	R/W	Delay flag of Bank A
8Ch	R/W	Sign bit of CSO
90h	RO	Bank A Current Sample Position Flag
94h	R/W	Current Envelope Buffer Control
98h	R/W	Bank A address engine interrupt
9Ch	R/W	Envelope engine interrupt register
A0h	R/W	Global Control & Channel Index
A4h	R/W	Bank A Address Engine Interrupt Enable
A8h	R/W	Global Music Volume & Global Wave Volume
ACh	R/W	Sample Change Step for Legacy Playback & Recording
B0h	R/W	Miscellaneous Int & Status
B4h	R/W	START command and status register for Bank B
B8h	R/W	Channel STOP command and status register for Bank B
BCh	RO	Bank B Current Sample Position Flag
C0h	R/W	Sound Blaster Base Block Length & Current Block

		Length
C4h	R/W	Sound Blaster Control
C8h	RO	Playback Sample Timer
D0h	R/W	Sample Timer Target
D8h	R/W	Bank B address engine interrupt
DCh	R/W	Bank B Address Engine Interrupt Enable
E0h	R/W	CSO & ALPHA & FMS
E4h	R/W	LBA
E8h	R/W	ESO & DELTA
ECh	R/W	Bank A LFO_CTRL & LFO_CT & FMC & RVOL & CVOL
ECh	R/W	Bank B ATTRIBUTE & FMC & RVOL & CVOL
F0h	R/W	Bank A GVSEL & PAN & VOL & CTRL & Ec
F0h		Bank B GVSEL & PAN & VOL & CTRL & Bank A LFO_INIT
F4h		EBUF1
F8h		EBUF2

7.8. AUTOMATIC POWER CONTROL (APC) REGISTERS

ADDRESS	ACCESS	REGISTER NAME
00h	R/W	APC Register 00h
01h	R/W	APC Register 01h
02h	R/W	APC Register 02h
03h	R/W	APC Register 03h
04h	R/W	APC Register 04h
05h	R/W	APC Register 05h

7.8.1. RTC REGISTERS

ADDRESS	ACCESS	REGISTER NAME
00h	R/W	Seconds
01h	R/W	Seconds Alarm
02h	R/W	Minutes
03h	R/W	Minutes Alarm
04h	R/W	Hours
05h	R/W	Hours Alarm
06h	R/W	Day of the Week
07h	R/W	Day of the Month
08h	R/W	Month
09h	R/W	Year
0Ah	R/W	Register A
0Bh	R/W	Register B (bit 3 must be set to 0)

0Ch	R/W	Register C
0Dh	R/W	Register D
7Eh	R/W	Day of the Month Alarm
7Fh	R/W	Month Alarm

8. REGISTER DESCRIPTION

8.1. LPC BRIDGE CONFIGURATION REGISTERS

DEVICE	IDSEL	FUNCTION NUMBER
LPC Bridge	AD12	0000b

Register 00h~01h Vendor ID

Default Value: 1039h

Access: Read Only

BIT	ACCESS	DESCRIPTION
15:0	RO	**Vendor Identification Number** Default value is 1039h

Register 02h~03h Device ID

Default Value: 0008h

Access: Read Only

BIT	ACCESS	DESCRIPTION
15:0	RO	**Device Identification Number** Default value is 0008h

Register 04h~05h Command Register

Default Value: 000Ch

Access: Read Only

BIT	ACCESS	DESCRIPTION
15:4	RO	**Reserved.** Read as 0
3	RO	**Read as 1 to indicate the device is allowed to monitor special cycles.**
2	RO	**Read as 1 to indicate the device is able to become PCI bus master.**
1	RO	**Response to Memory Space Accesses (default=0)** This bit is hard wired to1.
0	RO	**Response to Memory Space Accesses (default=0)** This bit is hard wired to 1.

Register 06h~07h Status

Default Value: 0200h

Access: Read Only

BIT	ACCESS	DESCRIPTION
15:14	RO	**Reserved.** Read as 0
13	RO	**Received Master-Abort** This bit will be set to 1 when the current transaction is terminated with master-abort. This bit can be cleared to 0 by writing a 1.
12	RO	**Received Target-Abort** This bit will be set to 1 when the current transaction is terminated with target-abort. This bit can be cleared to 0 by writing a 1.
11	RO	**Reserved.** Read as 0.
10:9	RO	**DEVSEL# Timing** The two bits are hardwired to 01 to indicate positive decode with medium timing.
8:0	RO	**Reserved.** Read as 0.

Register 08h Revision ID

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Revision Identification Number** Default value is 00h indicating the A0 stepping.

Register 09h~0Bh Class Code

Default Value: 060100h

Access: Read Only

BIT	ACCESS	DESCRIPTION
23:0	RO	**Class Code** Default value is 060100h.

Register 0Ch Cache Line Size

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION

7:0	RO	**Cache Line Size**

Register 0Dh Master Latency Timer

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Master Latency Timer**

Register 0Eh Header Type

Default Value: 80h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Header Type** Default value is 80h

Register 0Fh BIST

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**BIST** Default value is 00h

Register 10h~3Ch Reserved. Read as 0.

Register 40h BIOS Control Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**ACPI Enable** 0 : Disable 1 : Enable When enabled, ACPI register at IO space address as defined in ACPI base registers (Reg 74h~75h) can be accessed.
6:5	R/W	**Reserved.**
4	R/W	**PCI Posted Write Buffer Enable** 0 : Disable (default) 1 : Enable

3	R/W	**Subtractive Decode to Internal registers Enable** 0 : Disable 1 : Enable When this bit is enabled, the SiS960 will do subtractive decode on addresses for internal registers.
2	R/W	**Reserved.**
1	R/W	**BIOS positive Decode Enable** 0 : Disable 1 : Enable When enabled, SiS960 will positively respond to PCI memory cycles toward E segment and F segment. Otherwise, SiS960 will respond substractively.
0	R/W	**Extended BIOS Enable. (FFF80000~FFFDFFFF)** When enabled, SiS960 will positively respond to PCI cycles toward the Extended segment. Otherwise, SiS960 will have no response.

Register 41/42/43/44h PCI INTA#/B#/C#/D# Remapping Register

Default Value: 80/80/80/80h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Remapping enable** 0 : Disable 1 : Enable When enabled, PCI INTA#/B#/C#/D# will be remapped to the IRQ channel specified below.
6:4	RO	**Reserved.** Read as 0

3:0	R/W	**IRQ Remapping Table**					
		Bits	**IRQx#**	**Bits**	**IRQx#**	**Bits**	**IRQx#**
		0000	reserved	0110	IRQ6	1100	IRQ12
		0001	reserved	0111	IRQ7	1101	reserved
		0010	reserved	1000	Reserved	1110	IRQ14
		0011	IRQ3	1001	IRQ9	1111	IRQ15
		0100	IRQ4	1010	IRQ10		
		0101	IRQ5	1011	IRQ11		

Note: More than one of INT[A:D]# can be remapped to the same IRQ line, but that IRQ line should be programmed to level-triggered mode.

Register 45h Flash ROM Control Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:6	R/W	**Flash EPROM Control Bit** If bit 7 is set to '0' after CPURST de-asserted, EPROM can be flashed when bit 6 is set to '1'. Once bit 7 is set to '1', EPROM can not be flashed until the system is reset.
5:0	R/W	**Reserved.**

Register 46h INIT Enable Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:6	R/W	**Hardware reset initiated by software** When both set to 1, hardware reset will be generated to CPU.
5	R/W	**INIT Enable** 0 : Drives CPURST during S/W reset and INIT is inactive. 1 : Drives INIT during S/W reset
4	R/W	**Fast Gate 20 Emulation** 0 : Disable 1 : Enable

3	R/W	**Fast Reset Latency Control** 0 : 2us 1 : 6us
2	R/W	**Fast Reset Emulation** 0 : Disable 1 : Enable
1	R/W	**A20m# Output Control** 0 : Enable the assertion of A20M# if applicable. 1 : Disable the assertion of A20M#, i.e., A20M# will be high at all times.
0	R/W	**Enable Keyboard Hardware Reset** 0 : Disable 1 : Enable

Note: Write a 1 to Port 92 bit 0 will cause SiS960 to drive INIT if INIT Enable bit is 1, and Port 92 bit 1 will be set to 1 concurrently to Disable the assertion of A20M#.

Register 47h Keyboard Controller Register

Default Value: 50h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Reserved.**
6	R/W	**PS/2 Mouse Lock Enable** 0 : Disable 1 : Enable
5	R/W	**Internal Keyboard Controller Clock Selection** 0 : PCICLK/4 1 : 7.159MHz
4	R/W	**Keyboard Lock Enable** 0 : Disable 1 : Enable
3	R/W	**Integrated Keyboard Controller Enable** 0 : Disable 1 : Enable

2	R/W	**Integrated PS/2 Mouse Enable** 0 : Disable 1 : Enable This bit is meaningful only when Bit3 is enabled.
1	R/W	**Keyboard Hot Key Status** This bit is set when hot key (Ctrl+Alt+Backspace) is pressed and should be cleared at the end of SMI# handler. This bit is meaningful only when internal KBC is enabled.
0	R/W	**Keyboard Hot Key Control** 0 : Disable 1 : Enable This bit is meaningful only when internal KBC is enabled.

Register 48h RTC Control Register

Default Value: 10h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**RTC Extended Bank Enable (EXTEND_EN)** 0 : Disable 1 : Enable When this bit is enabled, the upper 128 bytes of RTC SRAM can be accessed.
6	R/W	**Automatic Power Control Registers (APCREG_EN) Enable** 0 : Disable 1 : Enable When this bit is enabled, APC registers can be accessed.
5	R/W	**Software Power Off System Control(SPWROFF)** Before enabling this function, the bit6 at APC Register 03h should be enabled. Once writing a 1 to this bit, system will be powered off.
4	RO	**Internal RTC Status** 0 : Disable 1 : Enable
3:0	R/W	**Reserved.**

Register 49h Individual Distributed DMA Channel Enable

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Channel 7 DDMA Enable**
6	R/W	**Channel 6 DDMA Enable**
5	R/W	**Channel 5 DDMA Enable**
4	R/W	**Reserved.** This bit must be programmed to 0.
3	R/W	**Channel 3 DDMA Enable**
2	R/W	**Channel 2 DDMA Enable**
1	R/W	**Channel 1 DDMA Enable**
0	R/W	**Channel 0 DDMA Enable** 0 : Disable 1 : Enable

Register 4A~4Bh Distributed DMA Master Configuration Register

Default Value: 0000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:4	R/W	**DDMA slave base address bits[15:4]** The DMA slave channels must be grouped into a 128 bytes block with 16 bytes per channel. The DMA slave channel 0 will be located at the base address specified here.
3:1	R/W	**Reserved.** This bit must be programmed to 0.
0	R/W	**DDMA Function Enable** 0 : Disable (default) 1 : Enable

Register 4C~4Fh Shadow Register of ICW1 to ICW4 of INT1

Default Value: 00000000h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Reflect ICW1 to ICW4 of the master interrupt controller**

Register 50~53h Shadow Register of ICW1 to ICW4 of INT2

Default Value: 00000000h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Reflect ICW1 to ICW4 of the slave interrupt controller**

Register 54~55h Shadow Register of OCW2 to OCW3 of INT1

Default Value: 0000h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Reflect OCW2 to OCW3 of the master interrupt controller**

Register 54~55h Shadow Register of OCW2 to OCW3 of INT2

Default Value: 0000h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Reflect OCW2 to OCW3 of the slave interrupt controller**

Register 58h CTC Shadow Register 1

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Reflect low byte of the initial count number of CTC Counter 0**

Register 59h CTC Shadow Register 2

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Reflect high byte of the initial count number of CTC Counter 0**

Register 5Ah CTC Shadow Register 3

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Reflect low byte of the initial count number of CTC Counter 1**

Register 5Bh CTC Shadow Register 4

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Reflect high byte of the initial count number of CTC Counter 1**

Register 5Ch CTC Shadow Register 5

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Reflect low byte of the initial count number of CTC Counter 2**

Register 5Dh CTC Shadow Register 6

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Reflect high byte of the initial count number of CTC Counter 2**

Register 5Eh CTC Shadow Register 7

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Reflect Control word (43h) of the built-in CTC**

Register 5Dh Shadow Register 8

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:6	RO	**Reserved.**
5	RO	**CTC counter2 Write count pointer status**
		CTC counter1 Write count pointer status
		CTC counter0 Write count pointer status
		CTC counter2 Read count pointer status
		CTC counter1 Read count pointer status

		CTC counter0 Read count pointer status 0 : LSB 1 : MSB

Register 60h Shadow Register for ISA port 70h

Default Value: FFh

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Reflect the content of ISA port 70h register**

Register 61h IDEIRQ Remapping Register

Default Value: 80h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**IDEIRQ Remapping Enable** 0 : Enable 1 : Disable (default)
6:5	R/W	**Reserved.**
4	R/W	**IDE Channel Remapping Selection** 0 : Primary IDE channel 1 : Secondary IDE channel
3:0	R/W	**IRQ Remapping Table**

Bits	IRQx#	Bits	IRQx#	Bits	IRQx#
0000	reserved	0110	IRQ6	1100	IRQ12
0001	reserved	0111	IRQ7	1101	reserved
0010	reserved	1000	reserved	1110	IRQ14
0011	IRQ3	1001	IRQ9	1111	IRQ15
0100	IRQ4	1010	IRQ10		
0101	IRQ5	1011	IRQ11		

Register 62h USBIRQ Remapping Register

Default Value: 80h

Access: Read/Write

BIT	ACCESS	DESCRIPTION

7	R/W	**USBIRQ Remapping Enable** 0 : Enable 1 : Disable (default)
6:4	R/W	**Reserved.**
3:0	R/W	**IRQ Remapping Table**

Bits	**IRQx#**	**Bits**	**IRQx#**	**Bits**	**IRQx#**
0000	reserved	0110	IRQ6	1100	IRQ12
0001	reserved	0111	IRQ7	1101	reserved
0010	reserved	1000	reserved	1110	IRQ14
0011	IRQ3	1001	IRQ9	1111	IRQ15
0100	IRQ4	1010	IRQ10		
0101	IRQ5	1011	IRQ11		

Register 63h GPEIRQ Remapping Register

Default Value: 80h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**GPEIRQ Remapping Enable** 0 : Enable 1 : Disable (default)
6:4	R/W	**Reserved.**
3:0	R/W	**IRQ Remapping Table**

Bits	**IRQx#**	**Bits**	**IRQx#**	**Bits**	**IRQx#**
0000	reserved	0110	IRQ6	1100	IRQ12
0001	reserved	0111	IRQ7	1101	reserved
0010	reserved	1000	reserved	1110	IRQ14
0011	IRQ3	1001	IRQ9	1111	IRQ15
0100	IRQ4	1010	IRQ10		
0101	IRQ5	1011	IRQ11		

Register 64h Priority Timer

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION

7:0	R/W	**Priority Timer** There are five PCI maser candidates inside SiS960 competing for the PCI bus. They are LPC/DMA master, MAC, DDMA with rotating priority and USB, Audio with fixed priority. The masters with fixed priority always have the higher priority than those with rotating priority. The candidate that issues request to the arbiter with a higher priority is the winner and is eligible to become PCI master when PHLDA# is received. The priority timer is used to set a lower limit in terms of PCI clock for the wining candidates with rotating priority to continue its PCI transactions. The timer will start counting as soon as the winning candidate with rotating priority receives PHLDA#. Upon expiration, the winning candidate's priority will become the lowest among the three with rotating priority and, if the requests issued by the other masters are outstanding, it will lose the ownership of PHLDA#. However, Even if the timer is not expired, the original winning candidates with rotating priority will be preempted by the masters with fixed priority asserting their requests. The maximum allowable value is FFh and the minimum allowable value is 00h.

Register 65h PHOLD# Timer

Default Value: 01h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	**PHOLD# Timer** The PHOLD# timer sets an upper limit in terms of PCI clock for the assertion time of PHOLD# initiated by LPC/DMA Master, MAC, DDMA, USB or Audio master. The timer starts and continues the counting when SiS960 receives PHLDA#. Upon expiration, the SiS960 will be forced to de-assert PHOLD#. The maximum allowable value is FFh and the minimum allowable value is 01h. If a larger value is programmed, the master will be able to complete more PCI transactions by preventing the system arbiter from issuing GNT# to other PCI master candidates. The PCI bus bandwidth can be fairly shared by all PCI master candidates by properly program this timer.

Register 66h Fixed Priority Selection

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:1	R/W	**Reserved.**

0	R/W	**Fixed Priority Selection** 0 : Audio has the higher priotiry than USB. (Default) 1 : USB has the higher priority than Audio.

Register 67h Clear SIRQ1 and SIRQ12

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**ISR bits clear SIRQ1 and SIRQ 12 Latches Enable** When set to 1, the internal latches for SIRQ1 and SIRQ12 will be cleared when the corresponding ISR bits are set in Interrupt Controller. The latches only take effective when either register 64h bit 7 or bit 6 is set to 1.The latches will always be cleared by a IO read cycle with address=60h.
6:5	R/W	**SMC37C673 SuperIO Compatible Mode** The two bits should be programmed to 1, if a SMC37C673 Super IO chip is connected to SiS5595 via serial IRQ line. Bit_6 enables the chipset to latch SIRQ1, while Bit_5 enables the chipset to latch SIRQ12. For all other super IO chips, the two bits should be programmed to 0
4	R/W	**Serial IRQ sampled IOCHK phase control** 0 : The sampled IOCHK on serial IRQ will be inverted. 1 : The sampled IOCHK on serial IRQ will not be inverted. (Recommended)
3:0	R/W	**Reserved.**

Register 68h USB & ACPI/SCI IRQ Remapping Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION				
7	R/W	**USB IRQ Remapping Enable** 0 : Disable (default) 1 : Enable				
6	R/W	**Reserved.**				
5:4	R/W	**IRQ Remapping Table**				
		Bits	00	01	02	03
		IRQx#	INTA#	INTB#	INTC#	INTD#

3	R/W	**ACPI/SCI IRQ Remapping Enable** 0 : Disable (default) 1 : Enable
2	R/W	**Reserved.**
1:0	R/W	**IRQ Remapping Table**

Bits	00	01	02	03
IRQx#	INTA#	INTB#	INTC#	INTD#

Register 69h AUDIO & MAC IRQ Remapping Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**AUDIO IRQ Remapping Enable** 0 : Disable (default) 1 : Enable
6	R/W	**Reserved.**
5:4	R/W	**IRQ Remapping Table**

Bits	00	01	02	03
IRQx#	INTA#	INTB#	INTC#	INTD#

3	R/W	**MAC IRQ Remapping Enable** 0 : Disable (default) 1 : Enable
2	R/W	**Reserved.**
1:0	R/W	**IRQ Remapping Table**

Bits	00	01	02	03
IRQx#	INTA#	INTB#	INTC#	INTD#

Register 6Ah ACPI/SCI IRQ Remapping Register

Default Value: 80h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**ACPI/SCI IRQ Remapping Enable** 0 : Enable 1 : Disable (default)

6:4	R/W	**Reserved.**
3:0	R/W	**IRQ Remapping Table**

Bits	**IRQx#**	**Bits**	**IRQx#**	**Bits**	**IRQx#**
0000	reserved	0110	IRQ6	1100	IRQ12
0001	reserved	0111	IRQ7	1101	reserved
0010	reserved	1000	reserved	1110	IRQ14
0011	IRQ3	1001	IRQ9	1111	IRQ15
0100	IRQ4	1010	IRQ10		
0101	IRQ5	1011	IRQ11		

Register 6Bh DEVICE BAY IRQ Remapping Register

Default Value: 80h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**DEVICE BAY IRQ Remapping Enable** 0 : Enable 1 : Disable (default)
6:4	R/W	**Reserved.**
3:0	R/W	**IRQ Remapping Table**

Bits	**IRQx#**	**Bits**	**IRQx#**	**Bits**	**IRQx#**
0000	reserved	0110	IRQ6	1100	IRQ12
0001	reserved	0111	IRQ7	1101	reserved
0010	reserved	1000	reserved	1110	IRQ14
0011	IRQ3	1001	IRQ9	1111	IRQ15
0100	IRQ4	1010	IRQ10		
0101	IRQ5	1011	IRQ11		

Register 6Ch SMBUS IRQ Remapping Register

Default Value: 80h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**SMBUS IRQ Remapping Enable** 0 : Enable 1 : Disable (default)

6:5	R/W	**Reserved.**
4	RO	**SMBus IRQ Status**
3:0	R/W	**IRQ Remapping Table**

Bits	**IRQx#**	**Bits**	**IRQx#**	**Bits**	**IRQx#**
0000	reserved	0110	IRQ6	1100	IRQ12
0001	reserved	0111	IRQ7	1101	reserved
0010	reserved	1000	reserved	1110	IRQ14
0011	IRQ3	1001	IRQ9	1111	IRQ15
0100	IRQ4	1010	IRQ10		
0101	IRQ5	1011	IRQ11		

Register 6Dh Software Watchdog IRQ Remapping Register

Default Value: 80h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Software Watchdog IRQ Remapping Enable** 0 : Enable 1 : Disable (default)
6:4	R/W	**Reserved.**
3:0	R/W	**IRQ Remapping Table**

Bits	**IRQx#**	**Bits**	**IRQx#**	**Bits**	**IRQx#**
0000	reserved	0110	IRQ6	1100	IRQ12
0001	reserved	0111	IRQ7	1101	reserved
0010	reserved	1000	Reserved	1110	IRQ14
0011	IRQ3	1001	IRQ9	1111	IRQ15
0100	IRQ4	1010	IRQ10		
0101	IRQ5	1011	IRQ11		

Register 6Eh Software-Controlled Interrupt Request, Channels 7-0

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Interrupt Channel 7**
6	R/W	**Interrupt Channel 6**

5	R/W	**Interrupt Channel 5**
4	R/W	**Interrupt Channel 4**
3	R/W	**Interrupt Channel 3**
2	R/W	**Interrupt Channel 2**
1	R/W	**Interrupt Channel 1**
0	R/W	**Interrupt Channel 0** Writing a 1 to these bits will cause the corresponding interrupt requests to be outstanding. This register defaults to all 0.

Register 6Fh Software-Controlled Interrupt Request, Channels 15-8

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Interrupt Channel 15**
6	R/W	**Interrupt Channel 14**
5	R/W	**Interrupt Channel 13**
4	R/W	**Interrupt Channel 12**
3	R/W	**Interrupt Channel 11**
2	R/W	**Interrupt Channel 10**
1	R/W	**Interrupt Channel 9**
0	R/W	**Interrupt Channel 8** Writing a 1 to these bits will cause the corresponding interrupt requests to be outstanding. This register defaults to all 0.

Register 70h Serial Interrupt Control Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Serial Interrupt (SIRQ) Control** 0 : Disable (default) 1 : Enable
6	R/W	**Quiet/Continuous Mode** 0 : Continuous (default) 1 : Quiet

5:2	R/W	**SIRQ Sample Period** 0000: 17 slots (default) 0001: 18 slots 0010: 19 slots :::::::::::: 1111: 32 slots
1:0	R/W	**Start Cycle length** 00: 4 PCI clocks (default) 01: 6 PCI clocks 10: 8 PCI clocks 11: Reserved

Register 71h Serial Interrupt Enable Register 1

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**INV-SIRQ**
6	R/W	**Serial SMI# Enable**
5	R/W	**Serial IOCHCK# Enable**
4	R/W	**Serial INTD Enable**
3	R/W	**Serial INTC Enable**
2	R/W	**Serial INTB Enable**
1	R/W	**Serial INTA Enable** 0 : Disable (default) 1 : Enable
0	R/W	**Reserved.**

Register 72h Serial Interrupt Enable Register 2

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Serial IRQ8 Enable**
6	R/W	**Serial IRQ7 Enable**

5	R/W	**Serial IRQ6 Enable**
4	R/W	**Serial IRQ5 Enable**
3	R/W	**Serial IRQ4 Enable**
2	R/W	**Serial IRQ3 Enable**
1	R/W	**Reserved.**
0	R/W	**Serial IRQ1 Enable** 0 : Disable (default) 1 : Enable

Register 73h Serial Interrupt Enable Register 3

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Reserved.**
6	R/W	**Serial IRQ15 Enable**
5	R/W	**Serial IRQ14 Enable**
4	R/W	**Serial IRQ13 Enable**
3	R/W	**Serial IRQ12 Enable**
2	R/W	**Serial IRQ11 Enable**
1	R/W	**Serial IRQ10 Enable**
0	R/W	**Serial IRQ9 Enable** 0 : Disable (default) 1 : Enable

Register 74~75h ACPI BASE Register

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:7	R/W	**ACPI Base Register A[15:7]** ACPI registers will be located at the address specified here.
6:0	RO	**Reserved.** Read as 0.

8.2 ACPI REGISTER

The following registers located at I/O base address <Base> + the indicated offset value <Offset>. The base address is programmed in the Register PCI Configuration space.

Register 00h~01h Power Management Status Register (PM1_STS)

Default Value: 0000h

Access: Read/Write Clear

The following registers are all sticky bits and only can be cleared by writing a one to their corresponding fields.

BIT	ACCESS	DESCRIPTION
15	R/WC	**Wake up Status (WAK_STS)** This bit is set when the system is in the sleeping state and an enabled wake-up event occurs. Upon setting this bit, the system will translate form sleep state to S0 state.
14:12	RO	**Reserved**
11	R/WC	**Ignored (Power Button Override Status)**
10	R/WC	**RTC Status (RTC_STS)** This bit is set when the RTC generates an IRQ8#. While both RTC_EN bit and RTC_STS bit are set, a power management event is raised.
9	RO	**Reserved**
8	R/WC	**Power Button Status (PWRBTN_STS)** This bit is set when the power button is pressed (the PWRBTN# signal is asserted Low). If PWRBTN_STS and PWRBTN_EN are both set under S0 state, then a SCI or SMI# is raised. If PWRBTN_STS bit is set under sleeping state, a WAKE event will be generated.
7:6	RO	**Reserved**
5	R/WC	**Global Status (GBL_STS)** This bit is set by a BIOS-initiated SCI. BIOS can initiate a SCI by writing a one to FIX_CNT bit 1.
4	R/WC	**Bus Master Status (BM_STS)** This is the bus master status bit. This bit is set when a system bus master is requesting the system bus.
3:1	RO	**Reserved**
0	R/WC	**Power Management Timer Status (PMTMR_STS)** This bit will be set if the MSB of PM_TMR is changed from '1' to '0' or '0' to '1'. While PMTMR_STS and PMTMR_EN bit are set, a power management event (SCI or SMI#) is raised.

Register 02h~03h Power Management Enable Register (PM1_EN)

Default Value: 0000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:11	RO	**Reserved**
10	R/W	**RTC Enable (RTC_EN)** This bit is used to enable the assertion of the RTC_STS to generate a power management event (Wake and SCI/SMI#).
9	RO	**Reserved**
8	R/W	**Power Button Enable (PWRBTN_EN)** This bit is used to enable the assertion of the PWRBTN_STS bit to generate a power management event (SCI/SMI#). The system always can wake up from Sx by Power Button regardless of the value of this bit.
7:6	RO	**Reserved**
5	R/W	**Global Enable (GBL_EN)** This bit is used to enable the assertion of the GBL_STS bit to generate a power management event (SCI).
4:1	RO	**Reserved**
0	R/W	**Power Management Timer Status (PMTMR_EN)** This is PMTMR enable bit. If this bit and PMTMR_STS bit are set, then a power management event is generated (SCI/SMI#).

Register 04h~05h Power Management Control Register (PM1_CNT)

Default Value: 0000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:14	RO	**Reserved**
13	WO	**Sleep Enable (SLP_EN)** This is a wirte only bit and always returns a zero when read. Setting this bit to one will cause the system to enter the sleep state defined by the SLP_TYP field.

12:10	R/W	**Sleeping Type (SLP_TYP)** Define the power-saving mode that the system should enter when the SLP_EN bit is set to one. 000 : S0 state (***Working***) 001 : S1 state (***STPCLK#***) 010 : S2 state (***STPCLK# and/or CPUSLP#***) 011 : S3 state (***Suspend To RAM***) 100 : S4 state (***Suspend To Disk***) 101 : S5 state (***Soft_Off***)
9:3	RO	**Reserved**
2	WO	**Global Release (GBL_RLS)** This bit is used by the ACPI software to raise a SMI# to the BIOS software. Writing a one to this register will generate a BIOS event to set BIOS_STS in LEG_STS.
1	R/W	**Bus Master Reload Enable (BM_RLD)** If enabled, a bus master request will cause any processor in the C3 state to transition to the C0 state. 0 : Disable 1 : Enable
0	R/W	**SCI Enable (SCI_EN)** Selects the power management event in PM1 to be either SCI or SMI#. When this bit is set, a power management event will generate SCI. When this bit is reset, a power management event will generate SMI#.

Register 06h~07h Reserved

Register 08h~0Bh ACPI Power Management Timer Register (PM_TMR)

Default Value: Free Running

Access: Read Only

BIT	ACCESS	DESCRIPTION
31:24	RO	**Reserved**
23:0	RO	**Power Management Timer Value** This read-only field reflects the current counting of the power management timer. The PM_TMR value will be reset when the system enter one of the sleeping state (S1~S5). Reading to this field will stop the running of PM_TMR.

Register 0Ch~0Fh Reserved

Register 10h~13h ACPI Processor Control Register (P_CNT)

Default Value: 0000 0000

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:5	RO	**Reserved**
4	R/W	**Throttling Function Enable** This bit enables the C0 clock throttling function.
3:1	R/W	**Throttling Duty Cycle Control** This 3-bit field determines the duty cycle of the STPCLK# signal when the system is in the C0 throttling mode. **Bits** — **Performance Rate** 000 — 100% 001 — 12.5% 010 — 25% 011 — 37.5% 100 — 50% 101 — 62.5% 110 — 75% 111 — 87.5%
0	RO	**Reserved**

Register 14h ACPI Processor Power State Level 2 (P_LVL2)

Default Value: 00

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Enter C2 Power State Register** Reading to this register returns all zeros; writes to this register have no effect. Reads to this register will also generate a " Enter C2 power state " event.

Register 15h ACPI Processor Power State Level 3 (P_LVL3)

Default Value: 00

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Enter C3 Power State Register** Reading to this register returns all zeros; writes to this register have no effect. Reads to this register will also generate a " Enter C3 power state " event.

Register 16h~19h Reserved

Register 1Ah~1Bh ACPI Fix Feature Control Register (FIX_CNT)

Default Value: 0040

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:10	RO	**Reserved**
9	R/W	**PM Timer Test Mode Enable** 0 : Disable 1 : Enable
8	R/W	**ACPI Fix Feature Test Mode Enable** 0 : Disable 1 : Enable
7	R/W	**PM1_STS Write Port Enable (PM1PORT_EN)** If this bit is enabled, writing a one to PM1_PORT register will cause the corresponding bit in PM1_STS to be set. 0 : Disable 1 : Enable
6	R/W	**Power Button Override Function Enable** When this bit is reset, the power button override function will be disabled. 0 : Disable 1 : Enable

5:4	R/W	**Power Button Trigger Mode Selection** The value in this field can select the trigger mode of power button. If the level mode is selected, PWRBTN_STS will always be set during the period of pressing power button. If the edge mode is selected, PWRBTN_STS can only be set once according to the power button is pressed or released. 00 : Level Mode 01 : Button press edge mode 10 : Button release edge mode 11 : Reserved
3	R/W	**CPUSLP# Enable** If this bit is set, CPUSLP# can be asserted for PII system to enter deep sleep state under S2. 0 : Disable 1 : Enable
2	RO	**Reserved**
1	WO	**BIOS Relationship (BIOS_RLS)** BIOS can set GBL_STS by writing a one to this field.
0	RO	**Reserved**

Register 1Ch~1Dh PM1_STS Write Port (PM1_PORT)

Default Value: 0000

Access: Write Only

BIT	ACCESS	DESCRIPTION
15:0	WO	**PM1_STS Write Port** Writing a one to this register will cause the corresponding field of PM1_STS to be set. Before writing to this register, PM1PORT_EN must be set.

Register 1Eh~1Fh Reserved

Register 20h~21h General Purpose Event 0 Status Register (GPE0_STS)

Default Value: 0000h

Access: Read/Write Clear

The following registers are all sticky bits and only can be cleared by writing a one to their corresponding fields. When one of status and their corresponding enable bits are set in S1/S2, a wakeup event is generated. If the status and the corresponding rerouting bits are set during working state (S0), an SCI/SMI#/IRQ will be generated. Note that IRQWAK_STS,

USBWAK_STS, and EXTSMIWAK_STS can only be set during sleeping state.

BIT	ACCESS	DESCRIPTION
15	R/WC	**IRQ Wake Status (IRQWAK_STS)** This bit is set when one of the enabled 8259 IRQ wakeup events is generated in S1/S2 state. Note: The IRQ wake-up events are defined in IRQWAK_CNT register.
14:13	RO	**Reserved**
12	R/WC	**MAC Power Management Event Status (MACPME_STS)** This bit is set when internal MAC power management event is generated.
11	R/WC	**PCI Power Management Event Status (PCIPME_STS)** This bit is set when PCI power management event is asserted for more than 4ms.
10	R/WC	**Device Bay Controller Status (DBC_STS)** This bit is set when an internal device bay controller event is generated due to DEVSTSCHG or REMBTN_STS is set. The 960 device bay controller must be enabled before using this bit.
9	R/WC	**Keyboard Controller Status (KBC_STS)** This bit is set when an internal keyboard controller hotkey event (CTRL+DEL+Backspace) is generated.
8	R/WC	**Ring Indication Status (RING_STS)** This bit is set when the RING goes active for more than 4ms. This bit can be choosed as quite or noise mode in GPECNT register. In quite mode, RING_STS can only be set during sleeping state (S1/S2). In noisy mode, RING_STS can be set in working and sleeping states.
7	R/WC	**SMBus Interrupt/I2C Alert Status (SMBINT_STS/I2CALT_STS)** If SMBus mode is selected, this bit will be set when a SMB interrupt is generated. If I2C mode is selected, this bit will be set when I2CALT# goes active.
6	RO	**Reserved**
5	R/WC	**Audio Controller Power Management Event Status (AUDPME_STS)** This bit is set when an internal AC'97 power management event is generated.
4	R/WC	**USB Wake Status (USBWAK_STS)** This bit is set when internal USB host controller detects a wake up event in sleeping state (S1/S2).
3	R/WC	**EXTSMI# Wake Status (EXTSMIWAK_STS)** This bit is set when EXTSMI# goes active in sleeping state (S1/S2).

2	R/WC	**EXTSMI# Status (EXTSMI_STS)** This bit is set when EXTSMI# goes active in working state (S0).
1	R/WC	**Thermal Event Override Status (THRMOR_STS)** This bit is set when THERM# goes active for more than 2 seconds. If THRMOR_DTY and THRMOR_THT are set, the system will enter thermal throttling mode.
0	R/WC	**Thermal Event Status (THRM_STS)** This bit is set when THERM# goes active.

Register 22h~23h General Purpose Event 0 Enable Register (GPE0_EN)

Default Value: 0000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15	R/W	**IRQ Wake Enable (IRQWAK_EN)**
14:13	RO	**Reserved**
12	R/WC	**MAC Power Management Event Enable (MACPME_EN)**
11	R/WC	**PCI Power Management Event Enable (PCIPME_EN)**
10	R/WC	**Device Bay Controller Enable (DBC_EN)**
9	R/WC	**Keyboard Controller Enable (KBC_EN)**
8	R/WC	**Ring Indication Enable (RING_EN)**
7	R/WC	**SMBus Interrupt/I2C Alert Enable (SMBINT_EN/I2CALT_EN)**
6	RO	**Reserved**
5	R/WC	**Audio Controller Power Management Event Enable (AUDPME_EN)**
4	R/WC	**USB Wake Enable (USBWAK_EN)**
3	R/WC	**EXTSMI# Wake Enable (EXTSMIWAK_EN)**
2	R/WC	**EXTSMI# Enable (EXTSMI_EN)**
1	R/WC	**Thermal Event Override Enable (THRMOR_EN)**
0	R/WC	**Thermal Event Enable (THRM_EN)**

Register 24h~27h General Purpose Event 0 Interrupt Routing Register (GPE0_ROUT)

Default Value: 0000 0000h

Access: Read/Write

The following registers are GPE0 routing registers. If one of GPE0_STS is set and its corresponding GPE0_ROUT register is routing to SCI/SMI#/GPEIRQ, an SCI/SMI#/GPEIRQ

will be generated.

BIT	ACCESS	DESCRIPTION
31:30	R/W	**IRQ Wake Route (IRQWAK_ROUT)** 00 : No effect 01 : SMI# 10 : SCI 11 : GPEIRQ
29:26	RO	**Reserved**
25:24	R/W	**MAC Power Management Event Route (MACPME_ROUT)**
23:22	R/WC	**PCI Power Management Event Route (PCIPME_ROUT)**
21:20	R/WC	**Device Bay Controller Route (DBC_ROUT)**
19:18	R/WC	**Keyboard Controller Route (KBC_ROUT)**
17:16	R/WC	**Ring Indication Route (RING_ROUT)**
15:14	R/WC	**SMBus/I2C Route (SMBINT_ROUT/I2CALT_ROUT)**
13:12	RO	**Reserved**
11:10	R/WC	**Audio Controller Power Management Event Route (AUDPME_ROUT)**
9:8	R/WC	**USB Wake Route (USBWAK_ROUT)**
7:6	R/WC	**EXTSMI# Wake Route (EXTSMIWAK_ROUT)**
5:4	R/WC	**EXTSMI# Route (EXTSMI_ROUT)**
3:2	R/WC	**Thermal Event Override Route (THRMOR_ROUT)**
1:0	R/WC	**Thermal Event Route (THRM_ROUT)**

Register 28h~29h General Purpose Event 0 Trigger Mode Selection (GPE0_TRG)

Default Value: 0000h

Access: Read/Write

If GPE0 is set to level trigger mode, the GPE0_STS will always be set by the active event as long as the event is not de-asserted. If GPE0_TRG is set to be edge trigger mode, the active event can only set GPE0_STS once before the active event is de-asserted.

BIT	ACCESS	DESCRIPTION
15	R/W	**IRQ Wake Trigger (IRQWAK_TRG)** 0 : Level trigger mode 1 : Edge trigger mode

14:13	RO	**Reserved**
12	R/W	**MAC Power Management Event Trigger (MACPME_TRG)**
11	R/WC	**PCI Power Management Event Trigger (PCIPME_TRG)**
10	R/WC	**Device Bay Controller Trigger (DBC_TRG)**
9	R/WC	**Keyboard Controller Trigger (KBC_TRG)**
8	R/WC	**Ring Indication Trigger (RING_TRG)**
7	R/WC	**SMBus/I2C Trigger (SMBINT_TRG/I2CALT_TRG)**
6	RO	**Reserved**
5	R/WC	**Audio Controller Power Management Event Trigger (AUDPME_TRG)**
4	R/WC	**USB Wake Trigger (USBWAK_TRG)**
3	R/WC	**EXTSMI# Wake Trigger (EXTSMIWAK_TRG)**
2	R/WC	**EXTSMI# Trigger (EXTSMI_TRG)**
1	R/WC	**Thermal Event Override Trigger (THRMOR_TRG)**
0	R/WC	**Thermal Event Trigger (THRM_TRG)**

Register 2Ah~2Bh General Purpose Event Control (GPE_CNT)

Default Value: 0000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:8	RO	**Reserved**
7	R/W	**GPE0_STS Write Port Enable (GPE0PORT_EN)** If this bit is enabled, writing a one to GPE0_PORT register will cause the corresponding bit in GPE0_STS to be set. 0 : Disable 1 : Enable
6	R/W	**RING Indication Quite/Noisy Mode Control (RING_CNT)** If RING is set to be quite mode, RING_STS can only be set in sleeping state (S1/S2). If the noisy mode is selected, RING_STS can be set in working and sleeping state. 0 : Noisy mode 1 : Quite mode

5	R/W	**SMBus/I2C Function Select (SMB_SEL)** If this bit is set to one, SMBDAT/I2CDAT, SMBCLK/I2CCLK, and SMBALT#/I2CALT# will be switched as I2C mode. Otherwise, they will be selected as SMBus mode. 0 : SMBus mode select 1 : I2C mode select
4	RO	**Reserved**
3	R/W	**Thermal Override Throttling Function Enable (THRMOR_THT)** This bit enables the thermal override throttling function. 0 : Disable 1 : Enable
2:0	R/W	**Thermal Override Throttling Duty Cycle Control** This 3-bit field determines the duty cycle of the STPCLK# signal when the thermal override event is generated. **Bits** — **Performance Rate** 000 — 100% 001 — 12.5% 010 — 25% 011 — 37.5% 100 — 50% 101 — 62.5% 110 — 75% 111 — 87.5%

Register 2Ch~2Dh GPE0_STS Write Port (GPE0_PORT)

Default Value: 0000

Access: Write Only

BIT	ACCESS	DESCRIPTION
15:0	WO	**GPE0_STS Write Port** Writing a one to this register will cause the corresponding field of GPE0_STS to be set. Before writing to this register, GPE0PORT_EN must be set.

Register 2Eh~2Fh Reserved

Register 30h~31h General Purpose Event 1 Status Register (GPE1_STS)

Default Value: 0000h

Access: Read/Write Clear

The following registers are all sticky bits and only can be cleared by writing a one to their corresponding fields. When one of status and their corresponding enable bits are set in S1/S2, a wakeup event is generated. If the status and the corresponding rerouting bits are set during working state (S0), an SCI/SMI#/IRQ will be generated. Not that if GPIO[n] are selected as output mode or their mux-ed function, their corresponding status bits must be ignored. So do their enable and route registers must be set to zero.

BIT	ACCESS	DESCRIPTION
15:0	R/WC	**GPIO[15:0] Status (GPIO[15:0]_STS)** This bit is set when one of GPIO[15:0] event goes active.

Register 32h~33h General Purpose Event 1 Enable Register (GPE1_EN)

Default Value: 0000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:0	R/W	**GPIO[15:0] Enable (GPIO[15:0]_EN)**

Register 34h~37h General Purpose Event 1 Interrupt Routing Register (GPE1_ROUT)

Default Value: 0000 0000h

Access: Read/Write

The following registers are GPE1 routing registers. If one of GPE1_STS is set and its corresponding GPE1_ROUT register is routing to SCI/SMI#/GPEIRQ, an SCI/SMI#/GPEIRQ will be generated.

BIT	ACCESS	DESCRIPTION
31:30	R/W	**GPIO15 Route (GPIO15_ROUT)** 00 : No effect 01 : SMI# 10 : SCI 11 : GPEIRQ
29:0	R/W	**GPIO[14:0] Route (GPIO[14:0]_ROUT)** See ths pattern of GPIO15_ROUT.

Register 38h~39h General Purpose Event 1 Trigger Mode Selection (GPE1_TRG)

Default Value: 0000h

Access: Read/Write

If GPE1 is set to level trigger mode, the GPE1_STS will always be set by the active event as

long as the event is not de-asserted. If GPE1_TRG is set to be edge trigger mode, the active event can only set GPE1_STS once before the active event is de-asserted.

BIT	ACCESS	DESCRIPTION
15:0	R/W	**GPIO[15:0] Trigger (GPIO[15:0]_TRG)** 0 : Level trigger mode 1 : Edge trigger mode

Register 3Ah~3Bh General Purpose Event 1 Pin Level (GPE1_LVL)

Default Value: 0000h

Access: Read/Write

If GPIO[n] is set to input mode, the input level of its corresponding GPIO pin can be read from this register. If GPIO[n] is set to output mode, the output level can be control through this register. Note that the output value of GPIO[n] must be written to this register before GPIO[n] is switch to output mode.

BIT	ACCESS	DESCRIPTION
15:0	R/W	**GPIO[15:0] Pin Level (GPIO[15:0]_LVL)** 0 : Pin input level low/Pin output level low 1 : Pin input level high/Pin output level high

Register 3Ch~3Dh General Purpose Event 1 Input/Output Mode Select (GPE1_IO)

Default Value: FFFFh

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:0	R/W	**GPIO[15:0] Input/Output Mode Select (GPIO[15:0]_IO)** 0 : Output Mode 1 : Input Mode

Register 3Eh~3Fh General Purpose Event 1 Input Polarity Select (GPE1_POL)

Default Value: 0000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:0	R/W	**GPIO[15:0] Input Polarity Select (GPIO[15:0]_POL)** 0 : Active low 1 : Active high

Register 40h~41h Legacy Event Status Register (LEG_STS)

Default Value: 0000h

Access: Read/Write Clear

The following registers are all sticky bits and only can be cleared by writing a one to their corresponding fields.

BIT	ACCESS	DESCRIPTION
15	R/WC	**Software Watch Dog Timer Event 1 Status (SFTMR1_STS)** This bit is set when the software watchdog timer expires the second time. This status bit does not have its corresponding enable bit and can survive under PCIRST#.
14	R/WC	**Software Watch Dog Timer Event 0 Status (SFTMR0_STS)** This bit is set when the software watchdog timer expires the first time. This status bit does not have its corresponding enable bit and can survive under PCIRST#.
13	R/WC	**General Purpose Event Status (GPESMI_STS)** This bit is set when the SMI# is caused by GPE0 or GPE1. This status bit does not have its corresponding enable bit.
12	R/WC	**Power Management Status (PM1SMI_STS)** This bit is set when the SMI# is caused by PM1. This status bit does not have its corresponding enable bit.
11:10	RO	**Reserved**
9	R/WC	**Serial IRQ SMI# Status (SIRQSMI_STS)** This bit is set when internal Serial IRQ decoder asserts an SMI#.
8	R/WC	**LPC SMI# Status (LPCSMI_STS)** This bit is set when internal LPC controller asserts an SMI#.
7	R/WC	**One Minute Status (ONEMIN_STS)** This bit is set every one minute. In legacy power management, ONEMIN_STS and ONEMIN_EN can be used to monitor the device status every one minute.
6	R/WC	**RTC Year 2000 Roll Over Status (RTCY2K_STS)** This bit is set when the 9th bit of RTC time register rolls from 99 to 00. This bit can be used to monitor the Y2K event.
5	R/WC	**SMI# Command Status (SMICMD_STS)** This bit is set when OS write a value to SMI# command port.
4	R/WC	**BIOS Status (BIOS_STS)** This bit is set when software write a one to GBL_RLS in PM1_CNT register.

3	R/WC	**Input/Output Trap 1 Status (IOTRAP1_STS)** This bit is set when software initiates an I/O access to the range of IOTRAP1_PORT and IOTRAP1_MASK
2	R/WC	**Input/Output Trap 0 Status (IOTRAP0_STS)** This bit is set when software initiates an I/O access to the range of IOTRAP0_PORT and IOTRAP0_MASK
1	R/WC	**Legacy USB Status (LEGUSB_STS)** This bit is set when a legacy USB SMI# is activated.
0	R/WC	**SMI# Status (SMI_STS)** This bit is set when one of the SMI# source is activated. The SMI# will be masked for 128 PCI clock after clearing this bit.

Register 42h~43h Legacy Event Enable Register (LEG_EN)

Default Value: 0000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:10	RO	**Reserved**
9	R/W	**Serial IRQ SMI# Enable (SIRQSMI_EN)**
8	R/W	**LPC SMI# Enable (LPCSMI_EN)**
7	R/W	**One Minute Enable (ONEMIN_EN)**
6	R/W	**RTC Year 2000 Roll Over Enable (RTCY2K_EN)**
5	R/W	**SMI Command Enable (SMICMD_EN)**
4	R/W	**BIOS Enable (BIOS_EN)**
3	R/W	**Input/Output Trap 1 Enable (IOTRAP1_EN)**
2	R/W	**Input/Output Trap 0 Enable (IOTRAP0_EN)**
1	R/W	**Legacy USB Enable (LEGUSB_EN)**
0	R/W	**SMI Enable (SMI_EN)**

Register 44h~45h Device Activity Status Register (DEVACT_STS)

Default Value: 0000h

Access: Read/Write Clear

The following registers are all sticky bits and only can be cleared by writing a one to their corresponding fields.

BIT	ACCESS	DESCRIPTION

15	R/WC	**Primary IDE Activity Status (IDEPACT_STS)** This bit is set when software initiates an I/O access to the range of 170h~177h and 376h.
14	R/WC	**Secondary IDE Activity Status (IDESACT_STS)** This bit is set when software initiates an I/O access to the range of 1F0h~1F7h and 3F6h.
13:12	RO	**Reserved**
11	R/WC	**Sound Blaster Activity Status (SBACT_STS)** This bit is set when software initiates an I/O access to the range of 220h~233h, 240h~253h, 260h~273h, and 280h~293h.
10	R/WC	**Microsoft Sound Activity Status (MSSACT_STS)** This bit is set when software initiates an I/O access to the range of 530h~537h, 604h~60Bh, E80h~E87h, and F40h~F47h.
9	R/WC	**MIDI Activity Status (MIDIACT_STS)** This bit is set when software initiates an I/O access to the range of 300h~303h, 310h~313h, 320h~323h, and 330h~333h.
8	R/WC	**Keyboard Controller Activity Status (KBCACT_STS)** This bit is set when software initiates an I/O access to the range of 60h and 64h.
7	R/WC	**Game Port Activity Status (GAMEACT_STS)** This bit is set when software initiates an I/O access to the range of 200h~207h and 388h~38Bh.
6	R/WC	**Floopy Activity Status (FLPYACT_STS)** This bit is set when software initiates an I/O access to the range of 3F0h~3F7h and 370h~377h.
5	R/WC	**Serial Port Activity Status (SERACT_STS)** This bit is set when software initiates an I/O access to the range of 2E8h~2EFh, 2F8h~2FFh, 3E8h~3EFh, and 3F8h~3FFh.
4	R/WC	**Parallel Port Activity Status (PARLACT_STS)** This bit is set when software initiates an I/O access to the range of 278h~27Fh, 378h~37Fh, and 3BCh~3BEh.
3	R/WC	**INTD# Activity Status (INTDACT_STS)** This bit is set when PCI INTD# goes active.
2	R/WC	**INTC# Activity Status (INTCACT_STS)** This bit is set when PCI INTC# goes active.
1	R/WC	**INTB# Activity Status (INTBACT_STS)** This bit is set when PCI INTB# goes active.

0	R/WC	**INTA# Activity Status (INTAACT_STS)** This bit is set when PCI INTA# goes active.

Register 46h~47h Reserved

Register 48h SMI# Command Port Register (SMICMD_PORT)

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	**SMI# Command Port Value** Writing to this register will generate an SMI# command event.

Register 49h Mail Box Register (MAIL_BOX)

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	**Read/Write Free Byte**

Register 4Ah Software Watchdog Timer Initial Value (SF_TMR)

Default Value: FFh

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	**Software Watchdog Timer Initial Value** Writing to this register will reload the software watchdog timer with the value specified in this register. If the software watchdog timer expires the first time, the expired event will set the SFTMR0_STS and the timer will reload its initial value and count again. If the timer expire the second time, the expired event will set the SFTMR1_STS.

Register 4Bh Software Watchdog Timer Control Register (SFTMR_CNT)

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Software Watchdog Timer Counting Enable** The software watchdog timer will start to count when this bit is set to one.
6	RO	**Reserved**

5:4	R/W	**Software Watchdog Timer Clock Select** 00 : 4ms 01 : 1sec 10 : 1min 11 : 1hour
3:2	R/W	**Software Watchdog Timer Expiration Event 1 Routing Select** When SFTMR1_STS is set to one, an SMI#/SFTIRQ/PCIRST# will be generated according to the following combination. 00 : No effect 01 : SMI# 10 : SFTIRQ 11 : PCIRST#
1:0	R/W	**Software Watchdog Timer Expiration Event 0 Routing Select** When SFTMR0_STS is set to one, an SMI#/SFTIRQ/PCIRST# will be generated according to the following combination. 00 : No effect 01 : SMI# 10 : SFTIRQ 11 : PCIRST#

Register 4Ch~4Fh High Resolution Timer Counting Value (HR_TMR)

Default Value: 0000 0000h

Access: Read Only

BIT	ACCESS	DESCRIPTION
31:0	RO	**High Resolution Timer Value** This read-only field reflects the current counting of HR_TMR. The clock source can be applied from MAC or AC'97. If this tmer is disabled, the counting value will be reset to zero. Note: The control register of PM_TMR is located in LEG_CNT.

Register 50h~51h Programmable 16-bits I/O Port Trap 0 Address (IOTRAP0_PORT)

Default Value: 0000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION

15:0	R/W	**I/O Port Trap 0 Address** Any I/O access to the range of IOTRAP0_PORT and IOTRAP0_MASK will cause IOTRAP0_STS to be set to one.

Register 52h~53h Programmable 16-bits I/O Port Trap 1 Address (IOTRAP1_PORT)

Default Value: 0000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:0	R/W	**I/O Port Trap 1 Address** Any I/O access to the range of IOTRAP1_PORT and IOTRAP1_MASK will cause IOTRAP1_STS to be set to one.

Register 54h Programmable 16-bits I/O Port Trap 0 Mask (IOTRAP0_MASK)

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	**I/O Port Trap 0 Mask** A one in this register will select the low 8-bit mask for IOTRAP0_PORT.

Register 55h Programmable 16-bits I/O Port Trap 1 Mask (IOTRAP1_MASK)

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	**I/O Port Trap 0 Mask** A one in this register will select the low 8-bit mask for IOTRAP1_PORT.

Register 56h~57h Legacy Event Control (LEG_CNT)

Default Value: 0040h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:8	RO	**Reserved**

7	R/W	**LEG_STS Write Port Enable (LEGPORT_EN)** If this bit is enabled, writing a one to LEG_PORT register will cause the corresponding bit in LEG_STS to be set. 0 : Disable 1 : Enable
6	R/W	**Auto Reset Enable (AUTORST_EN)** If this bit is enabled and ROMCS# is pulled low, a PCIRST# will generate every 4~5 seconds. 0 : Disable 1 : Enable
5:4	RO	**Reserved**
3:2	R/W	**High Resolution Timer Clock Source Select** 00 : MAC 25MHz/25 (1MHz) 01 : Reserved 10 : AC' 97 12.288MHz/12 (1024KHz) 11 : AC' 97 12.288MHz/16 (768KHz)
1	R/W	**High Resolution Timer Counting Enable** If HR_TMR is disabled, the HR_TMR value will be reset to zero. 0 : Disable 1 : Enable
0	R/W	**SMI# Mask Interval Select** If SMI_STS is cleared, the SMI# will be masked a certain time according to this register. 0 : 128 PCICLK 1 : 8 PCICLK

Register 58h~59h LEG_STS Write Port (LEG_PORT)

Default Value: 0000h

Access: Write Only

BIT	ACCESS	DESCRIPTION
15:0	WO	**LEG_STS Write Port** Writing a one to this register will cause the corresponding field of LEG_STS to be set. Before writing to this register, LEGPORT_EN must be set.

Register 5Ah~5Bh IRQ and NMI Enable for Wake-up Event Control (IRQWAK_CNT)

Default Value: 0000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:3	R/W	**Correspond to the enable bits for IRQ[15:3] to generate a wake-up event**
2	R/W	**Correspond to the enable bits for NMI to generate a wake-up event**
1:0	R/W	**Correspond to the enable bits for IRQ[1:0] to generate a wake-up event**

Register 5Ch~5Dh I/O Address Track for SMI# (ADDR_TRACK)

Default Value: 0000h

Access: Read Only

BIT	ACCESS	DESCRIPTION
15:0	RO	**I/O Address Track** The reading value in this register reflects the address of last I/O cycle from CPU before the system enter SMI# handler.

Register 5Eh I/O Command/Byte Enable Track for SMI# (CBE_TRACK)

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:4	RO	**I/O Byte Enable Track** The reading value in this register reflects the byte enable of last I/O cycle from CPU before the system enter SMI# handler.
3:0	RO	**I/O Command Track** The reading value in this register reflects the command of last I/O cycle from CPU before the system enter SMI# handler.

Register 5Fh I2C Control Register (I2C_CNT)

Default Value: 1Fh

Access: Read/Write, Read Only

BIT	ACCESS	DESCRIPTION
7:5	RO	**Reserved**
4	RO	**I2CALT# Pin Level (I2CALT_LVL)** The reading value in this register reflects the input level of I2CALT#.

3	RO	**I2CDAT Pin Level (I2CDAT_LVL)** The reading value in this register reflects the input level of I2CDAT.
2	RO	**I2CCLK# Pin Level (I2CCLK_LVL)** The reading value in this register reflects the input level of I2CCLK.
1	R/W	**I2CDAT Pin Output Level (I2CDAT_OUT)** A zero in this field will force I2CDAT pin to output low level. A one in this field will make this pin floating.
0	R/W	**I2CCLK Pin Output Level (I2CCLK_OUT)** A zero in this field will force I2CCLK pin to output low level. A one in this field will make this pin floating.

Register 60h~61h System Wakeup form S3/S4/S5 Status Register (S5WAK_STS)

Default Value: 0000h

Access: Read Only

The following registers are all located in resume well. They can survive as long as the stanby power exists. The only way to clear the register is to write S5WAK_CLR or deassert AUXOK.

BIT	ACCESS	DESCRIPTION
15	RO	**Power Button Wakeup Status (PWRBTN_S5WAK_STS)** This bit will be set if power button wakes up the system from S3/S4/S5.
14	RO	**RTC Wakeup Status (RTC_S5WAK_STS)** This bit will be set if a RTC IRQ8# wakes up the system from S3/S4/S5.
13	RO	**RING Wakeup Status (RING_S5WAK_STS)** This bit will be set if RING wakes up the system from S3/S4/S5.
12	RO	**MACPME Wakeup Status (MACPME_S5WAK_STS)** This bit will be set if MAC power management event wakes up the system from S3/S4/S5.
11	RO	**PCIPME Wakeup Status (PCIPME_S5WAK_STS)** This bit will be set if PCI power management event wakes up the system from S3/S4/S5.
10	RO	**AUDPME Wakeup Status (AUDPME_S5WAK_STS)** This bit will be set if AC'97 power management event wakes up the system from S3/S4/S5.
9	RO	**Keyboard Password/Hotkey Wakeup Status (KBC_S5WAK_STS)** This bit will be set if keyboard password or hotkey wakes up the system from S3/S4/S5.

8	RO	**USB Wakeup Status (USB_S5WAK_STS)** This bit will be set if USB wakes up the system from S3/S4/S5.
7	RO	**SMBALT# Wakeup Status (SMBALT_S5WAK_STS)** This bit will be set if SMBALT# wakes up the system from S3/S4/S5.
6	RO	**Power Supply Resume to Previous State Status (RSM_S5WAK_STS)** This bit will be set if power supply resume function wakes up the system from S5.
5:2	RO	**Reserved**
1	RO	**System Suspend to DRAM State Status (S3OFF_STS)** This bit will be set if the system enters to S3 state.
0	RO	**Reserved**

Register 62h~63h System Wakeup form S3/S4/S5 Control Register (S5WAK_CNT)

Default Value: 0000h

Access: Read/Write

The following registers are all located in resume well. They can survive as long as the stanby power exists.

BIT	ACCESS	DESCRIPTION
15:12	RO	**Wake Block Counter Reading** These bits are testing registiers and only for internal use.
11:10	RO	**Reserved**
9	R/W	**Wake Block Counter Test Enable** 0 : Disable 1 : Enable
8	R/W	**Wake Block Function Test Enable** 0 : Disable 1 : Enable

7:6	R/W	**ACPILED Output State Control** The output state of ACPILED can be controlled by the following combination when system is in S0/S1/S2/S3 states. If the system is in S4/S5 state, ACPILED will be set to high impedience. 00 : Output low 01 : Blink 10 : High impedience 11 : Reserved
5:1	RO	**Reserved**
0	R/W	**S5WAK_STS Clear Status (S5WAK_CLR)** If this register is set to one, all register in S5WAK_STS will be reset to zero.

Register 64h~7Fh Reserved

Register 80h SMBus Status (SMB_STS)

Default Value: 00h

Access: Read/Write Clear

The following registers are all sticky bits and only can be cleared by writing a one to their corresponding fields.

BIT	ACCESS	DESCRIPTION
7	R/WC	**SMBus Slave Alert (SMBALT_STS)** This bit is set when the SMBALT# is active.
6	R/WC	**HIT SLAVE Alias Address (SMBALIAS_STS)** This bit is set when the Host Slave received a Write Word from a device master and the address field match the Slave Alias Address register. If this bit is set to one, on more Write Word transaction can be received by SMBus Slave until this bit is cleared to zero.
5	R/WC	**HIT Host Slave (SMBSLAVE_STS)** This bit is set when the Host Slave received a Write Word from a device master and the address field is 10h. . If this bit is set to one, on more Write Word transaction can be received by SMBus Slave until this bit is cleared to zero.

4	R/WC	**Block Array (SMBARY_STS)** This bit is set when he SMBus Host has finished 8 bytes transition for Block Protocol. If the byte count of the Block protocol is 32, then total 4 Interrupt request will occur during the entire block transition. For the first three Interrupt, the service TRGine should program the following 8 data bytes as soon as possible, or the total trasnfer time may violate SMBus SPEC 1.0 (Timeout < 10ms). After the next eight bytes data are programmed to the SMB_BYTE0~7, the service TRGine should clear this status bit to initiate the following block transition.
3	R/WC	**Host Master (SMBMAS_STS)** This bit is set when the SMBus Host Master transition is complete.
2	R/WC	**SMBus Collision (SMBCOL_STS)** This bit is set when a SMBus Collision condition occurs and SMBus Host loses in the bus arbitration. The software should clear this bit and re-start SMBus operation.
1	R/WC	**Device Error (SMBERR_STS)** This bit is set when a Device Error condition occur. The Device Errors may cause by: Host asserts an unclaimed slave address/data. Host detects a Slave Timeout –may be a Slave error condition Slave detects a Master Timeout
0	RO	**SMBus Interrupt Status (SMBINTR_STS)** A one in this field incicates a SMBus interrupt is generated by any of above Interrupt source.

Register 81h SMBus Enable (SMB_EN)

Default Value: 00h

Access: Read/Write

A SMBus Interrupt can be generated if Register 81h, bit 0 is enabled and the Interrupt Status bit with associated enable bits are set to one.

BIT	ACCESS	DESCRIPTION
7	R/W	**SMBus Slave Alert Interrupt Enable (SMBALT_EN)** When this bit is enabled, a SMBus Interrupt will be generated by the active SMBALERT#. 0 : Disable 1 : Enable

6	R/W	**SMBus Slave Alias Address Interrupt Enable(SMBALIAS_EN)** When this bit is enabled and the Device Address field of the Write Word Protocol received by Host Slave match the Slave Alias Address, a SMBus Interrupt will be generated. 0 : Disable 1 : Enable
5	R/W	**SMBus Slave Interrupt Enable(SMBSLAVE_EN)** When this bit is enabled and the Device Address field of the Write Word Protocol received by Host Slave is 10h, a SMBus Interrupt will be generated. 0 : Disable 1 : Enable
4	R/W	**Block Array Interrupt Enable (SMBARY_EN)** When this bit is enabled and the Host Master has finished 8 bytes transition for Block Protocol, a SMBus Interrupt will be generated. 0 : Disable 1 : Enable
3	R/W	**Host Master Interrupt Enable (SMBMAS_EN)** When this bit is enabled and the Host Master transition is complete, a SMBus Interrupt will be generated. 0 : Disable 1 : Enable
2	R/W	**SMBus Collision Interrupt Enable (SMBCOL_EN)** 0 : Disable 1 : Enable
1	R/W	**Device Error Interrupt Enable (SMBERR_EN)** 0 : Disable 1 : Enable
0	R/W	**SMBus Interrupt Enable (SMBINTR_EN)** This bit is used to enable the SMBus interrupt generation. 0 : Disable 1 : Enable

Register 82h SMBus Control (SMB_CNT)

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Host Slave Timeout Enable (SLTO_EN)** When this bit is enabled and the Host Slave transition time is over specification, a SMBus Interrupt will be generated. 0 : Disable 1 : Enable
6	R/W	**Host Master Timeout Enable (MSTO_EN)** When this bit is enabled and the Host Master transition time is over specification, a SMBus Interrupt will be generated. 0 : Disable 1 : Enable
5	R/W	**SMBus Host Master Clock Selection (SMBCLK_SEL)** 0 : 14KHz 1 : 56KHz
4:2	RO	**Reserved**
1	R/W	**Slave Busy (SL_BUSY)** Indicate the Host Slave is in idle or active state**.** 1 : Active 0 : Idle
0	R/W	**Host Busy (HOST_BUSY)** Indicate the Host Master is in idle or active state**.** When Host Master is in IDLE state, the Host Master is free for software to control. 1 : Active 0 : Idle

Register 83h SMBus Host Control (SMBHOST_CNT)

Default Value: 00h

Access: Write Only, Read/Write

BIT	ACCESS	DESCRIPTION
7:6	RO	**Reserved**
5	WO	**Kill (SMB_Kill)** This bit is set to stop all SMBus operation, including Host master and slave, all activities are set to initial state. This operation won't effect the values in R/W registers.

4	WO	**Start (SMB_START)** Writing a 1 to this bit which initiate the SMBus Host transition. The SMBus Command Protocaol bits (SMB_PTL) and the associated registers should be properly programmed before this bit is set to 1. This is a write-only bit.
3	R/W	**Reserved**
2:0	R/W	**SMBus Command Protocol (SMB_PTL)** Selecting the Protocol that SMBus Host is going to execute. Reading or Writing transition is determined by SMBus Address register bit 0 (R/W bit). **Bit[3:1]** — **Protocol** 000 — Quick command 001 — Send/Receive Byte 010 — Read/Write Byte Data 011 — Read/Write Word Data 100 — Process Call 101 — Read/Write Block Data 110 — Reserved 111 — Reserved

Register 84h SMBus Address (SMB_ADDR)

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:1	R/W	**SMBus Address (SMB_ADDRESS)** The field is the slave address to target device.
0	R/W	**SMBus Read/Write (SMB_RW)** 1 : Execute a read protocol 0 : Execute a write protocol This bit doesn't effect Process Call protocol.

Register 85h SMBus Command (SMB_CMD)

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION

7:0	R/W	**SMBus Command (SMB_COMMAND)** This register contains the command code and will be sent to device.

Register 86h SMBus Processed Byte Count (SMB_PCOUNT)

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:5	RO	**Reserved**
4:0	RO	**SMBus Processed Byte Count (SMB_PCNT)** The field is the byte count that Host has transferred for block protocol. The SMBus Interrupt TRGine can read this register to know how many bytes are not transferred yet when the SMB_CNT is over 8 bytes. A 'zero' indicates a maximun of 32 data bytes has transferred.

Register 87h SMBus Byte Count (SMB_COUNT)

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:5	RO	**Reserved**
4:0	R/W	**SMBus Byte Count(SMB_CNT)** The field is the byte count for Block Read/Write protocol. The byte count can not be 0.

Register 88h~8Fh SMBus Byte0~7 (SMB_BYTE0~7)

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	**SMBus Byte0~7 (SMB_BYTE0~7)** These seven bytes are the data byte field for Block Read/Write protocol. The Byte0 is also used in Byte protocol, including Received Byte, Read/Write Data Byte protocol. In addition, the Byte0 (low byte) and Byte1 (high byte) are combined as word during word protocol, including Read/Write Word, Process Call protocol.

Register 90h SMBus Device Address (SMBDEV_ADDR)

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	**SMBus Device Address (SMBDEV_ADDR)** This field stores the Device Address when Host Slave received a Write Word protocol from other SMBus master.

Register 91h SMBus Device Byte0 (SMB_DB0)

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	**SMBus Device Byte 0 (SMB_DB0)** This field stores the Data Low Byte when Host Slave received a Write Word protocol from other SMBus master.

Register 92h SMBus Device Byte1 (SMB_DB1)

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	**SMBus Device Byte 1 (SMB_DB1)** This field stores the Data High Byte when Host Slave received a Write Word protocol from other SMBus master.

Register 93h SMBus Host Slave Alias Address (SMB_SAA)

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:1	R/W	**SMBus Host Slave Alias Address (SMB_ALIAS)** When Host Slave receives a Device Address the same as the address in these seven bits and bit 0 is '0', an interrupt will be raised if Alias Interrupt is also enabled.
0	R/W	Read as '0'. The Host Slave accepts master Write Word protocol only.

Register 94h~9Fh Reserved

Register A0~A1h DBC Vender ID

Default Value: 1039h

Access: Read Only

BIT	ACCESS	DESCRIPTION

15:0	RO	**Vendor Identification Number** Default value is 1039h.

Register A2h~A3h Reserved

Register A4h DBC Revision ID

Default Value: A0h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	**Revision Identification Number** Default value is A0h indicating A0 stepping.

Register A5h~ABh Reserved

Register ACh~AFh DBC Capabilities Register (DBCCR)

Default Value: 0000 0002h

Access: Read Only

BIT	ACCESS	DESCRIPTION
31:5	RO	**Reserved**
4	RO	**Security Lock Support (SECLOCK)** Default value is 0.
3:0	RO	**Bay Count (BAYCNT[3:0])** Default value is 02h.

Register B0h~B3h Bay 0 Status Register (BSTR0)

Default Value: 0000 0000h

Access: Read Only, Read/Write Clear

BIT	ACCESS	DESCRIPTION
31:11	RO	**Reserved**
10:8	RO	**The Form Factor of the Bay 0 (BAY0_FF[2:0])** Default value is 000 (DB32 form factor).
7	RO	**Reserved**

6:4	RO	**The Actual State of the Bay 0 (BAY0_ST[2:0])** The bay 0 states are decoded as follows: **BAY0_ST[2:0]** — **Meaning** 000 — Bay Empty 001 — Device Inserted 010 — Device Enabled 011 — Removal Requested 100 — Device Removal Allowed 101 — Reserved 110 — Reserved 111 — Reserved
3	R/WC	**Removal Request Button Status For Bay 0 (REMREQ0_STS)** This bit is set when the removal button is pressed and a device is present in the bay. When both REMREQ0_STS and REMREQ0_EN are set, an interrupt can be generated within DBC. This is a sticky bit and can only be reset by writing a one to this field.
2	R/WC	**Device Status Change Indication Bit (DEVSTSCHG0)** This bit is set when the state of either of the presence pins for bay 0 transitions. When both DEVSTSCHG0_EN and DEVSTSCHG0 are set, an interrupt can be generated within DBC. This is a sticky bit and can only be reset by writing a one to this field.
1	RO	**1394 Device Presence For Bay 0 (1394PRSN0_STS)** If a 1394 device is present on bay 0, then this bit will be set to 1. If no 1394 device is present on this bay, this bit will be set to 0.
0	RO	**USB Device Presence For Bay 0 (USNPRSN0_STS)** If a USB device is present on bay 0, then this bit will be set to 1. If no USB device is present on this bay, this bit will be set to 0.

Register B4h~B7h Bay 0 Control and Enable Register (BCER0)

Default Value: 0000 0000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:8	RO	**Reserved**
7	R/W	**Bay 0 Software Controlled Interlock Control (LOCK0_CNT)** When set to 1, the bay 0 software controlled interlock is enable. When cleared to 0, the interlock mechanism is disabled.

6:4	R/W	**The Bay 0 State Requested by Operating System (BAY0_STREQ[2:0])** This field represents the state of bay 0 as requested by the operating system. **BAY0_STREQ[2:0]** — **Meaning** 000 — No Change 001 — Change State to Device Inserted 010 — Change State to Device Enabled 011 — Change State to Removal Requested 100 — Change State to Device Removal Allowed 101 — No Effect 110 — No Effect 111 — No Effect
3	R/W	**Remval Button Request for Bay 0 Enable (REMREQ0_EN)** When set to 1, an internal DBC interrupt due to a remval button request event will be enabled.
2	R/W	**Device Status Change Event Enable (DEVSTSCHG0_EN)** When set to 1, an internal DBC interrupt due to a device status change event will be enabled.
1	R/W	**Device Remove Event Wakeup Enable (REMEVTWAK0_EN)** When set to 1, an device removal event will be cause DEVSTSCHG0 to be set when the bay 0 is in state 100b. When set to 0, device removal events when the bay 0 is in state 100b will not cause DEVSTSCHG0 to be set.
0	R/W	**Bay 0 Power Control (PWR0_CTL)** When set to 1, bay 0 Vid power is enabled. When set to 0, bay 0 Vid power is disabled.

Register B8h~BCh Bay 1 Status Register (BSTR1)

Default Value: 0000 0000h

Access: Read Only, Read/Write Clear

BIT	ACCESS	DESCRIPTION
31:11	RO	**Reserved**
10:8	RO	**The Form Factor of the Bay 1 (BAY1_FF[2:0])** Default value is 000 (DB32 form factor).
7	RO	**Reserved**

6:4	RO	**The Actual State of the Bay 1 (BAY1_ST[2:0])** The bay 1 states are decoded as follows: **BAY1_ST[2:0]** — **Meaning** 000 — Bay Empty 001 — Device Inserted 010 — Device Enabled 011 — Removal Requested 100 — Device Removal Allowed 101 — Reserved 110 — Reserved 111 — Reserved
3	R/WC	**Removal Request Button Status For Bay 1 (REMREQ1_STS)** This bit is set when the removal button is pressed and a device is present in the bay. When both REMREQ1_STS and REMREQ1_EN are set, an interrupt can be generated within DBC. This is a sticky bit and can only be reset by writing a one to this field.
2	R/WC	**Device Status Change Indication Bit (DEVSTSCHG1)** This bit is set when the state of either of the presence pins for bay 1 transitions. When both DEVSTSCHG1_EN and DEVSTSCHG1 are set, an interrupt can be generated within DBC. This is a sticky bit and can only be reset by writing a one to this field.
1	RO	**1394 Device Presence For Bay 1 (1394PRSN1_STS)** If a 1394 device is present on bay 1, then this bit will be set to 1. If no 1394 device is present on this bay, this bit will be set to 0.
0	RO	**USB Device Presence For Bay 1 (USNPRSN1_STS)** If a USB device is present on bay 1, then this bit will be set to 1. If no USB device is present on this bay, this bit will be set to 0.

Register BCh~BFh Bay 1 Control and Enable Register (BCER1)

Default Value: 0000 0000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:8	RO	**Reserved**
7	R/W	**Bay 1 Software Controlled Interlock Control (LOCK1_CNT)** When set to 1, the bay 1 software controlled interlock is enable. When cleared to 0, the interlock mechanism is disabled.

6:4	R/W	**The Bay 1 State Requested by Operating System (BAY1_STREQ[2:0])** This field represents the state of bay 1 as requested by the operating system. **BAY1_STREQ[2:0]** — **Meaning** 000 — No Change 001 — Change State to Device Inserted 010 — Change State to Device Enabled 011 — Change State to Removal Requested 100 — Change State to Device Removal Allowed 101 — No Effect 110 — No Effect 111 — No Effect
3	R/W	**Remval Button Request for Bay 1 Enable (REMREQ1_EN)** When set to 1, an internal DBC interrupt due to a remval button request event will be enabled.
2	R/W	**Device Status Change Event Enable (DEVSTSCHG1_EN)** When set to 1, an internal DBC interrupt due to a device status change event will be enabled.
1	R/W	**Device Remove Event Wakeup Enable (REMEVTWAK1_EN)** When set to 1, an device removal event will be cause DEVSTSCHG1 to be set when the bay 1 is in state 100b. When set to 0, device removal events when the bay 1 is in state 100b will not cause DEVSTSCHG0 to be set.
0	R/W	**Bay 1 Power Control (PWR1_CTL)** When set to 1, bay 1 Vid power is enabled. When set to 0, bay 1 Vid power is disabled.

8.3 APC REGISTER

The following registers located at RTC power well. Before access to these registers, the APCRAM_EN must be set to one and EXPRAM_EN must be set to zero.

Register 00h CPU Frequency and Power Supply Resume Control

Default Value: 04h

Access: Read/Write

BIT	ACCESS	DESCRIPTION			
7:4	R/W	**Multiplication of CPU Core Frequency to Bus Frequency**			
		0000 : 2/1	0100 : 5/2	1000 : 6/1	1100 : 13/2
		0001 : 3/1	0101 : 7/2	1001 : 7/1	1101 : 15/2
		0010 : 4/1	0110 : 9/2	1010 : 8/1	1110 : 3/2
		0011 : 5/1	0111 : 11/2	1011 : Rev	1111 : 2/1
3	R/W	**CPU Frequency Ratio Control Selection** 0 : By Hardware Trap 1 : By bit7~4 of this register			
2	R/W	**Jumperless Reset Counter Enable** If CPU frequency ratio is selected as jumperless setting, the jumperless reset counter will start to count while PWROK goes active. When the counter expired, the CPU frequency ratio will be switched to hardware trap setting. 0 : Disable 1 : Enable			
1:0	R/W	**Power Supply ON/OFF State Resume Control** The value in this field determines the power supply state once the standby is suddenly off. 00 : Always Off 01 : Reserved 10 : Always On 11 : Keep previous state			

Register 01h MAC and RTC Test Mode Enable

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**MAC Serial ROM Autoload Function Enable** 0 : Disable 1 : Enable

6	R/W	**MII Test Mode Enable** This bit is only for internal use. 0 : Disable 1 : Enable
5	R/W	**RING Input/Output Mode Control** This bit is only for internal use. 0 : Input Mode 1 : Output Mode
4	R/W	**RING Input Polarity Control** 0 : Active high 1 : Active low
3:0	R/W	**RTC 32KHz Oscillator Circuit Test Mode Control** These bits are only for internal use.

Register 02h Mux-ed Function Select

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**Legacy ROM/Device Bay Interface Select** 0 : Legacy ROM interface select 1 : Device Bay interface select
6	R/W	**PHY/MII Interface Select** 0 : PHY interface select 1 : MII interface select
5	R/W	**GPIO9/CKES# Function Select** 0 : GPIO9 function select 1 : CKES# function select
4	R/W	**GPIO8/SPDIF Function Select** 0 : GPIO8 function select 1 : SPDIF function select
3	R/W	**GPIO[7:6]/MIDI Function Select** 0 : GPIO[7:6] function select 1 : MIDI function select

2	R/W	**GPIO5/SMBALT# Function Select** 0 : GPIO5 function select 1 : SMBALT# function select
1:0	R/W	**GPIO[4:0]/KBC/OC[4:0]# Function Select** 00 : GPIO[4:0] function select 01 : Reserved 10 : KBC function select 11 : OC[4:0]# function select

Register 03h Audio and USB Wakeup Enable

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**CODEC1 Wake from S3/S4/S5 Enable (CODEC1_S5WAK_EN)** 0 : Disable 1 : Enable
6	R/W	**CODEC0 Wake from S3/S4/S5 Enable (CODEC0_S5WAK_EN)** 0 : Disable 1 : Enable
5	R/W	**AUDPME Wake from S3/S4/S5 Enable (AUDPME_S5WAK_EN)** 0 : Disable 1 : Enable
4	R/W	**USB Port4 Wake from S3/S4/S5 Enable (USB4_S5WAK_EN)** 0 : Disable 1 : Enable
3	R/W	**USB Port3 Wake from S3/S4/S5 Enable (USB3_S5WAK_EN)** 0 : Disable 1 : Enable
2	R/W	**USB Port2 Wake from S3/S4/S5 Enable (USB2_S5WAK_EN)** 0 : Disable 1 : Enable
1	R/W	**USB Port1 Wake from S3/S4/S5 Enable (USB1_S5WAK_EN)** 0 : Disable 1 : Enable

0	R/W	**USB Port0 Wake from S3/S4/S5 Enable (USB0_S5WAK_EN)** 0 : Disable 1 : Enable

Register 04h System Power-Off Control

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:2	R/W	**Reserved**
1	R/W	**ACPI S5 Function Enable (S5OFF_EN)** 0 : Disable 1 : Enable
0	R/W	**ACPI S3 Function Enable (S3OFF_EN)** 0 : Disable 1 : Enable

Register 05h GPE Wakeup Enable

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	**RTC IRQ8 Wake from S3/S4/S5 Enable (RTC_S5WAK_EN)** 0 : Disable 1 : Enable
6	R/W	**RING Wake from S3/S4/S5 Enable (RING_S5WAK_EN)** 0 : Disable 1 : Enable
5	R/W	**MACPME Wake from S3/S4/S5 Enable (MACPME_S5WAK_EN)** 0 : Disable 1 : Enable
4	R/W	**PCIPME Wake from S3/S4/S5 Enable (PCIPME_S5WAK_EN)** 0 : Disable 1 : Enable

3	R/W	**SMBALT# Wake from S3/S4/S5 Enable (SMBALT_S5WAK_EN)** 0 : Disable 1 : Enable
2	R/W	**Keyboard Password Wake from S3/S4/S5 Enable (KBPS_S5WAK_EN)** 0 : Disable 1 : Enable
1	R/W	**Keyboard Hotkey Wake from S3/S4/S5 Enable (KBHK_S5WAK_EN)** 0 : Disable 1 : Enable
0	R/W	**Keyboard 8MHz Clock Shutdown** 0 : Clock Running 1 : Clock shutdown

8.4 10M/100M ETHERNET CONTROLLER REGISTERS

SiS900 is configured and controlled through registers. There are three categories of control/status registers implemented inside SiS900, which includes PCI Configuration Registers, MAC Operational Registers and MII PHY Registers. The PCI Configuration registers are mapped into PCI configuration space and accessed using PCI configuration bus cycles. The MAC Operational registers can be mapped into either PCI memory or PCI IO space. MII PHY Registers are accessed through MAC Operational Register ENPHY (ENhanced PHY access register, offset 1Ch). SiS900 requires an allocation of 256 bytes of operational register space, and 72 bytes of PCI configuration register space. The detailed definitions for each bit allocated in each registers will be described in section 4.2, 4.3 and 4.4 respectively.

Acronyms mentioned in the PCI configuration registers and MAC Operational registers are defined as follows:

RO Read Only

R/W Read Write

Acronyms mentioned in the MII PHY registers that are defined as follows:

SYM.	NAME	DEFINITION	
		WRITE CYCLE	READ CYCLE
W	Write	Input	No Operation
R	Read	No Operation	Output
R/W	Read/Write	Input	Output

R/WSC	Read/Write Self Cleaning	Input	Output Clears itself After Operation Complete
R/LL	Read/Latching Low	No Operation	Output When Bit Goes Low, Bit Latched. When Bit is Read, Bit Updated.
R/LH	Read/Latching High	No Operation	Output When Bit Goes High, Bit Latched. When Bit is Read, Bit Updated.
R/LT	Read/Latching on Transition	No Operation	Output When Bit Transitions, Bit Latched And Interrupt Set When Bit is Read, Interrupt Clear And Bit Updated.

8.5 PCI CONFIGURATION REGISTERS

SiS900 implements a PCI version 2.1 configuration register space. This allows PCI BIOS to "soft" configure SiS900. Software Reset has no effect on configuration registers. Hardware Reset returns all configuration registers to their hardware reset state. For all reserved registers, a write are ignored, and a read return 0.

Table 4-1 Configuration Register Map

OFFSET	TAG	DESCRIPTION	ACCESS	SECTION
00h	CFGID	Configuration Identification Register	RO	4.2.1
04h	CFGCS	Configuration Command and Status Register	R/W	4.2.2
08h	CFGRID	Configuration Revision ID Register	RO	4.2.3
0Ch	CFGLAT	Configuration Revision ID Register	R/W	4.2.4
10h	CFGIOA	Configuration IO Base Address Register	R/W	4.2.5
14h	CFGMA	Configuration Memory Address Register	R/W	4.2.6
18h-28h		RESERVED (reads return zero).		
2Ch	CFGSID	Configuration Subsystem Identification Register	RO	4.2.7
30h	CFGEROMA	Configuration Expansion ROM Base Address Register	R/W	4.2.8

34h	CFGCAP	Configuration Capabilities Pointer Register	RO	4.2.9
38h		RESERVED (reads return zero).		
3Ch	CFGINT	Configuration Interrupt Select Register	R/W	4.2.10
40h	CFGPMC	Configuration Power Management Capabilities Register	RO	4.2.11
44h	CFGPMCSR	Configuration Power Management Control and Status Register	R/W	4.2.12
48-FFh		RESERVED (reads return zero).		

Register 00h Configuration Identification

Default Value: 09001039h

Access: Read Only

This register identifies SiS900 to PCI system software.

BIT	ACCESS	DESCRIPTION
31:16	RO	**Device ID** This field is read-only and is set to the device ID 0900h assigned by SiS if auto load is not enabled. If auto load is enabled, it is set to the device ID stored in Serial EEPROM.
15:0	RO	**Vendor ID** This field is read-only and is set to a value of 1039h that is SiS's PCI Vendor ID if auto load is not enabled. If auto load is enabled, it is set to the vendor ID stored in EEPROM.

Register 04h Configuration Command and Status

Default Value: 02900000h

Access: Read/Write

This register has two parts. The upper 16-bits (31-16) is devoted to device status. The lower 16-bits (15-0) is devoted to command and are used to configure and control the device.

BIT	ACCESS	DESCRIPTION
31	R/W	**Detected Parity Error** SiS900 sets this bit whenever a parity error is detected, even if the parity error handling is disabled (controlled by command register bit 6). SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
30	R/W	**Signaled SERR** This bit is set whenever SiS900 asserts SERR#. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
29	R/W	**Received Master Abort** SiS900 sets this bit whenever its master transaction is terminated with Master-Abort. SW writes '0' to this bit leaves this bit unchanged.
28	R/W	**Received Target Abort** SiS900 sets this bit whenever its master transaction is terminated with Target-Abort. SW writes '0' to this bit leaves this bit unchanged.

27	R/W	**Sent Target Abort** SiS900 sets this bit whenever it terminates a target transaction with Target-Abort. SW writes '0' to this bit leaves this bit unchanged.
26:25	RO	**DEVSEL Timing** This field will always be set to 01 indicating that SiS900 supports "medium" DEVSEL timing.
24	R/W	**Data Parity Detected** This bit is set when three conditions are met: (1) the bus agent asserted PERR# itself or observed PERR# asserted; (2) SiS900 acted as the bus master for the operation in which the error occurred; and (3) the Parity Error Response bit in command register is set. SW writes '0' to this bit leaves this bit unchanged.
23	RO	**Fast Back-to-Back Capable** SiS900 will set this bit to 1.
22	RO	**User Definable Features Supported** SiS900 do not support User Definable Features, and therefore reads will return a 0.
21	RO	**66MHz Capable** SiS900 is not 66MHz capable. Reads will return a 0.
20	RO	**Capabilities** SiS900 will set this bit to 1 indicating implementation of extended capabilities (PCI power management).
19:10		**Reserved** Reads return 0.
9	R/W	**Fast Back-to-Back Enable** Set to 1 by the PCI BIOS to enable SiS900 to do Fast Back-to-Back transfers (FBB transfers as a master is not implemented in the current revision).
8	R/W	**SERR# Enable** When set, SiS900 will generate SERR# when an address parity error is detected.
7	RO	**Address Data Stepping** This bit is hardwired to 0 for SiS900 never do stepping.
6	R/W	**Parity Error Response** When set, SiS900 will assert PERR# on the detection of a data parity error when acting as the target, and will sample PERR# when acting as the initiator. When reset, data parity errors are ignored. The action taken is specified by CFG: PESEL.

5	RO	**VGA Palette Snoop** SiS900 does not implement this bit. Reads will return a 0.
4	RO	**Memory Write and Invalidate Enable** Set to 0 indicating that SiS900 will not generate the Memory Write and Invalidate command.
3	RO	**Special Cycles** Set to 0 indicating that SiS900 will ignore all Special Cycle operations.
2	R/W	**Bus Master Enable** When set, SiS900 is allowed to act as a PCI bus master. When reset, SiS900 is prohibited from acting as a PCI bus master.
1	R/W	**Memory Space Access** When set, SiS900 responds to memory space accesses. When reset, SiS900 ignores memory space accesses.
0	R/W	**IO Space Access** When set, SiS900 responds to IO space accesses. When reset, SiS900 ignores IO space accesses.

Register 08h Configuration Revision ID

Default Value: 02000001h

Access: Read Only

This register stores silicon revision number, revision number of software interface specification and lets the configuration software know that it is an Ethernet controller in the class of network controllers.

BIT	ACCESS	DESCRIPTION
31:24	RO	**Base Class** Returns 02 which specifies a network controller.
23:16	RO	**Sub Class** Returns 00, which specifies an Ethernet controller.
15:8	RO	**Programming IF** Returns 00, which specifies the first release of SiS900 Software Interface Specification.
7:0	RO	**Silicon Revision** Returns 01, which specifies the silicon revision.

Register 0Ch Configuration Latency Timer

Default Value: 00000000h

Access: Read/Write

This register gives status and controls such miscellaneous functions as BIST, Latency timer and Cache line size.

BIT	ACCESS	DESCRIPTION
31:24	RO	**Built-in Self Test** SiS900 do not support BIST. Read will return 0, write is ignored.
23:16	RO	**Header Type** 00h
15:8	R/W	**Latency Timer** Set by software to the number of PCI clocks that SiS900 may hold the PCI bus.
7:0	RO	**Cache Line Size** Ignored by SiS900.

Register 10h Configuration IO Base Address

Default Value: 00000001h

Access: Read/Write

This register specifies the Base I/O address that is required to build an address map during configuration. It also specifies the number of bytes required as well as an indication that it can be mapped into I/O space.

BIT	ACCESS	DESCRIPTION
31:8	R/W	**Base IO Address** This is set by software to the base IO address for the Operational Register Map.
7:2	RO	**Size indication** Read back as 0. This allows the PCI bridge to determine that SiS900 requires 256 bytes of IO space.
1		**Reserved** Reads return 0.
0	RO	**IO Space Indicator** Set to 1 by SiS900 to indicate that SiS900 is capable of being mapped into IO space.

Register 14h Configuration Memory Address

Default Value: 00000000h

Access: Read/Write

This register specifies the Base Memory address that is required to build an address map during configuration. It also specifies the number of bytes required as well as an indication that it can be mapped into memory space.

BIT	ACCESS	DESCRIPTION
31:12	R/W	**Memory Base Address** This is set by software to the base address for the Operational Register Map.
11:4	RO	**Memory Size** These bits return 0, which indicates that SiS900 requires 4096 bytes of Memory Space (the minimum recommended allocation)
3	RO	**Prefetchable** Set to 0 by SiS900 to indicate that SiS900 does not support this feature.
2:1	RO	**Location Selection** Set to 00 by SiS900. This indicates that the base register is 32-bits wide and can be placed anywhere in the 32-bit memory space
0	RO	**Memory Space Indicator** Set to 0 by SiS900 to indicate that SiS900 is capable of being mapped into memory space.

Register 2Ch Configuration Subsystem Identification

Default Value: 09001039h

Access: Read Only

This register allows system software to distinguish between different subsystems based on the same PCI silicon.

BIT	ACCESS	DESCRIPTION
31:16	RO	**Subsystem Device ID** This field is set to the device ID 0900h assigned by SiS if auto load is not enabled. If auto load is enabled, it is set to the subsystem ID stored in EEPROM.
15:0	RO	**Subsystem Vendor ID** This field is set to a value of 1039h, which is SiS' s PCI Vendor ID if auto load is not enabled. If auto load is enabled, it is set to the subvendor ID stored in EEPROM.

Register 30h Configuration Expansion ROM Base Address

Default Value: 00000000h

Access: Read/Write

This register specifies the Base Expansion ROM address that is required to build an address map during configuration. It also specifies the number of bytes required as well as an indication that the device accepts accesses to its expansion ROM.

BIT	ACCESS	DESCRIPTION
31:17	R/W	**Expansion ROM Base Address** This is set by software to the base address for the Expansion ROM.
16:1		**Reserved** Reads return 0.
0	R/W	**Expansion ROM address decode enable** This SiS900 will respond to access its expansion ROM when this bit is set and the Memory Space Access bit is set.

Register 34h Configuration Capabilities Pointer

Default Value: 00000040h

Access: Read Only

BIT	ACCESS	DESCRIPTION
31:8		**Reserved** Reads return 0.
7:0	RO	**Capabilities Pointer** It provides an offset into PCI configuration space for the location of the first item in the capabilities linked list. Hardwired to 40' h in SiS900 to point to CFGPMC.

Register 3Ch Configuration Interrupt Select

Default Value: 0b340100h

Access: Read/Write

This register stores the interrupt line number as identified by the POST software that is connected to the interrupt controller as well as SiS900 desired settings for maximum latency and minimum grant.

BIT	ACCESS	DESCRIPTION
31:24	RO	**Maximum Latency** SiS900 desired setting for Max Latency. SiS900 will initialize this field to 0B (2.75 µsec).
23:16	RO	**Minimum Grant** SiS900 desired setting for Minimum Grant. SiS900 will initialize this field to 34 (13 µsec).
15:8	RO	**Interrupt Pin** Always return 0000 0001 (INTA).

7:0	R/W	**Interrupt Line** Set to which line on the interrupt controller that SiS900's interrupt pin is connected to.

Register 40h Configuration Power Management Capabilities

Default Value: fe010001h

Access: Read Only

SiS900 supports both PCI Bus Power Management Interface specifications. revision 1.0 and revision 1.0a. If auto load is enabled, the CFGPMC register is 1.0a version, otherwise it is 1.0 version.

1.0 version:

BIT	ACCESS	DESCRIPTION
31:27	RO	**PME Support** Indicates PME# may be asserted from which power state. If Auxiliary Power Source is present, this 5-bit field is 11111b indicating PME# can be asserted from D0, D1, D2, D3hot and D3cold. If Auxiliary Power Source is absent, this 5-bit field is 01111b indicating PME# can be asserted from D0, D1, D2 and D3hot but cannot be asserted from D3cold.
26	RO	**D2 Support** Set to 1 by SiS900 to indicate that SiS900 supports D2 Power Management State.
25	RO	**D1 Support** Set to 1 by SiS900 to indicate that SiS900 supports D1 Power Management State.
24:22		**Reserved** Reads return 0.
21	RO	**Device Specific Initialization** Set to 0 by SiS900 to indicate that SiS900 does not require a device specific initialization sequence following transition to the D0 uninitialized state.
20		**Reserved** Reads return 0.
19	RO	**PME Clock** Set to 0 by SiS900 to indicate that no PCI clock is required for SiS900 to generate PME#.
18:16	RO	**PCI PM Spec. Version** Set to 001b indicates that SiS900 complies with Revision 1.0 of the PCI Power Management Interface Specification.

15:8	RO	**Next Item Pointer** Set to 00h by SiS900 to indicate that no additional items in the Capabilities List.
7:0	RO	**Capability ID** Set to 01h by SiS900 to indicate that the linked list item as being the PCI Power Management registers.

1.0a version:

BIT	ACCESS	DESCRIPTION
31:27	RO	**PME Support** Indicates PME# may be asserted from which power state. If Auxiliary Power Source is present, this 5-bit field is 11111b indicating PME# can be asserted from D0, D1, D2, D3hot and D3cold. If Auxiliary Power Source is absent, this 5-bit field is 01111b indicating PME# can be asserted from D0, D1, D2 and D3hot but cannot be asserted from D3cold.
26	RO	**D2 Support** Set to 1 by SiS900 to indicate that SiS900 supports D2 Power Management State.
25	RO	**D1 Support** Set to 1 by SiS900 to indicate that SiS900 supports D1 Power Management State.
24:22	RO	**Auxiliary Current** This field reports the 3.3Vaux auxiliary current requirements for SiS900.
21	RO	**Device Specific Initialization** Set to 0 by SiS900 to indicate that SiS900 does not require a device specific initialization sequence following transition to the D0 uninitialized state.
20		**Reserved** Reads return 0.
19	RO	**PME Clock** Set to 0 by SiS900 to indicate that no PCI clock is required for SiS900 to generate PME#.
18:16	RO	**PCI PM Spec. Version** Set to 010b indicates that SiS900 complies with Revision 1.0a of the PCI Power Management Interface Specification.

15:8	RO	**Next Item Pointer** Set to 00h by SiS900 to indicate that no additional items in the Capabilities List.
7:0	RO	**Capability ID** Set to 01h by SiS900 to indicate that the linked list item as being the PCI Power Management registers.

Register 44h Configuration Power Management Control/Status

Default Value: 00000000h

Access: Read/Write

This register is used to manage SiS900's power management state as well as to enable/monitor PME

BIT	ACCESS	DESCRIPTION
31:24	RO	**State Dependent Data** Not implemented in SiS900 (reads return 0).
23:16	RO	**PMCSR PCI to PCI Bridge Support Extensions** Not implemented in SiS900 (reads return 0).
15	R/W	**PME Status** This bit is set when SiS900 would normally assert the PME# signal independent of the state of the PME_EN bit. Writing a '1' to this bit will clear it and cause SiS900 to stop asserting a PME# (if enabled). Writing a '0' has no effect. If Auxiliary Power Source is present, i.e. PME# can be asserted from D3cold, then this bit must be explicitly cleared by the operating system each time the operating system is initially loaded. Unchanged by hardware reset.
14:13	RO	**Data Scale** Not implemented in SiS900 (reads return 0).
12:9	RO	**Data Select** Not implemented in SiS900 (reads return 0).
8	R/W	**PME Enable** Writing a '1' enables SiS900 to assert PME#. Writing a '0', PME# assertion is disabled. If Auxiliary Power Source is present, i.e. PME# can be asserted from D3cold, then this bit must be explicitly cleared by the operating system each time the operating system is initially loaded. Unchanged by hardware reset.
7:2		**Reserved** Reads return 0

1:0	R/W	**Power State** This 2-bit field is used both to determine the current power state of SiS900 and to set SiS900 into a new power state. The hardware reset value is 00b. The definition of the field values is given below. 00b D0 01b D1 10b D2 11b D3hot

8.6 MAC OPERATIONAL REGISTERS

8.7 MAC OPERATIONAL REGISTERS

SiS900 provides the following set of operational registers mapped into PCI memory space or I/O space. Writes to reserved register locations may result in unexpected behavior. Reads to reserved register locations will return unspecified value.

Table 4-2 Operational Register Map

REGISTER	TAG	DESCRIPTION	ACCESS	SECTION
00h	CR	Command Register	R/W	4.3.1
04h	CFG	Configuration Register	R/W	4.3.2
08h	EROMAR	EEPROM Access Register	R/W	4.3.3
0Ch	PTSCR	PCI Test Control Register	R/W	4.3.4
10h	ISR	Interrupt Status Register	R/W	4.3.5
14h	IMR	Interrupt Mask Register	R/W	4.3.6
18h	IER	Interrupt Enable Register	R/W	4.3.7
1Ch	ENPHY	Enhanced PHY Access Register	R/W	4.3.8
20h	TXDP	Transmit Descriptor Pointer Register	R/W	4.3.9
24h	TXCFG	Transmit Configuration Register	R/W	4.3.10
28-2Ch		RESERVED		
30h	RXDP	Receive Descriptor Pointer Register	R/W	4.3.11
34h	RXCFG	Receive Configuration Register	R/W	4.3.12
38h	FLOWCTL	Flow Control Register	R/W	4.3.13
3C-44h		RESERVED		
48h	RFCR	Receive Filter Control Register	R/W	4.3.14

4Ch	RFDR	Receive Filter Data Register	R/W	4.3.15
50-ACh		RESERVED		
B0h	PMCTL	Power Management Control Register	R/W	4.3.16
B4h	PMEVT	Power Management Wake-up Event Register	R/W	4.3.17
B8h		RESERVED		
BCh	WAKECRC	Wake-up Sample Frame CRC Register	R/W	4.3.18
C0-ECh	WAKEMASK	Wake-up Sample Frame Mask Registers	R/W	4.3.19
F0-FCh		RESERVED		

Register 00h Command

Default Value: 00000000h

Access: Read/Write

This register is used for issuing commands to SiS900. These commands are issued by setting the corresponding bits for the function. Global software reset along with individual reset and enable/disable switches for transmitter and receiver are provided here.

BIT	ACCESS	DESCRIPTION
31-9		**Reserved**
8	R/W	**Reset** Set to 1 to force SiS900 to a soft reset state, which disables the transmitter and receiver, reinitializes the FIFOs, and resets all affected registers to their soft reset state. This operation implies both a TXR and a RXR. This bit will read back a 1 during the reset operation, and be cleared to 0 by the hardware when the reset operation is complete.
7	R/W	**Software Interrupt** Setting this bit to a 1 forces SiS900 to generate a hardware interrupt. This interrupt is maskable via the IMR.
6		**Reserved**
5	R/W	**Receiver Reset** When set to a 1, this bit causes the current packet reception to be aborted, the receiver data and status FIFOs to be flushed, and the receiver state machine to enter the idle state (RXE goes to 0). This is a write-only bit and is always read back as 0.

4	R/W	**Transmit Reset** When set to a 1, this bit causes the current transmission to be aborted, the transmitter data and status FIFOs to be flushed, and the transmitter state machine to enter the idle state (TXE goes to 0). This is a write-only bit and is always read back as 0.
3	R/W	**Receiver Disable** Disable the receiver's state machine after any current packets in progress. When this operation has been completed the RXE bit will be cleared to 0. This is a write-only bit and is always read back as 0. If the programmer is silly enough to set both RXD and RXE in the same write, the RXE will be ignored, and RXD will have precedence.
2	R/W	**Receiver Enable** When set to a 1, and the receiver's state machine is idle, then the receiver's machine becomes active. This bit will read back as a 1 whenever the receive state machine is active. After initial power-up, software must insure that the receiver has completely reset before setting this bit (see ISR:RXRCMP)
1	R/W	**Transmit Disable** When set to a 1, halts the transmitter after the completion of the current packet. This is a write-only bit and is always read back as 0. If the programmer is silly enough to set both TXD and TXE in the same write, the TXE will be ignored, and TXD will have precedence.
0	R/W	**Transmit Enable** When set to a 1, and the transmit state machine is idle, then the transmit state machine becomes active. This bit will read back as a 1 whenever the transmit state machine is active. After initial power-up, software must insure that the transmitter has completely reset before setting this bit (see ISR:TXRCMP)

Register 04h Configuration

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31-8		**Reserved**
7	R/W	**PCI Bus Request Algorithm** Selects mode for making requests for the PCI bus. When set to 0 (default), SiS900 will use an aggressive Request scheme. When set to a 1, SiS900 will use a more conservative scheme.

6	R/W	**Single Backoff** Setting this bit to 1 forces the transmitter backoff state machine to always backoff for a single 802.3 slot time instead of following the 802.3 random backoff algorithm. 0 (default) allows normal transmitter backoff operation.
5		**Program Out of Window Timer** This bit controls when the Out of Window collision timer begins counting its 512-bit slot time. A 0 causes the timer to start after the SFD is received. A 1 causes the timer to start after the first bit of the preamble is received.
4	R/W	**Excessive Deferral Timer disable** Setting this bit to 1 will inhibit transmit errors due to excessive deferral. This will inhibit the setting of the ED status.
3	R/W	**Parity Error Detection Action** This bit control the assertion of SERR when a data parity error is detected while SiS900 is acting as the bus master. When set, parity errors will not result in the assertion of SERR. When reset, parity errors will result in the assertion of SERR, indicating a system error.
2-1		**Reserved**
0	R/W	**Big Endian Mode** When set, SiS900 will perform bus-mastered data transfers in "big endian" mode. Note that access to register space is unaffected by the setting of this bit.

Register 08h Serial EEPROM Access

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31-4		**Reserved**
3	R/W	**EEPROM Chip Select** Controls the value of the EECS pin. When set, the EECS pin is 1; when clear the EECS pin is 0.
2	R/W	**EEPROM Serial Clock** Controls the value of the EESK pin. When set, the EESK pin is 1; when clear the EESK pin is 0.
1	RO	**EEPROM Data Out** Returns the current state of the EEDO/PA2 pin when EECS is 1. When EECS is 0, this bit returns 0.

0	R/W	**EEPROM Data In** Controls the value of the EEDI pin.

Register 08h PCI Test Control

Default Value: 34000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31		**Reserved**
30	R/W	**Discard Timer Test Mode** Setting this bit to 1, the discard timer for delay transaction will have an initial value of 3ff0h. Setting this bit to 0, the initial value of the discard timer will be 0 and the counter expires when up-count to 3fffh. Default value is set to 0.
29-28		**Reserved**
27-24	R/W	**Boot ROM Access Time** This field adjusts the boot ROM access time. The default value is 0100b that equal to 4 PCI clocks.
23-21		**Reserved**
20-12	R/W	**TX/RX RAM address** Used as the address for the Transmit/Receive data FIFO when accessed through TXCFG/RXCFG during RAM test mode.
11-10		**Reserved**
9	R/W	**Bus Master Test Enable** When enabled (set to 1), the bus master test mode allows the TX buffer manager to be used as a bus master read cycle generator, and the RX buffer manager to be used as a bus master write cycle generator. While in this test mode, normal buffer manager operation is inhibited. The BMTEN bit should only be set to 1 after the TX and RX have been reset and disabled. After setting BMTEN to 0, the TX and RX must be reset and reconfigured to allow normal operation to resume.
8		**Reserved**
7	R/W	Receive RAM Test Mode Enable Set this bit to 1 to enable Receive RAM Test mode, which will allow read/write access to the RX data FIFO. The address is specified in bit20-12 RAM address field. The data is written to or read from the RXCFG register.

6	R/W	**Transmit RAM Test Mode Enable** Set this bit to 1 to enable Transmit RAM Test mode, which will allow read/write access to the TX data FIFO. The address is specified in bit20-12 RAM address field. The data is written to or read from the TXCFG register.
5	R/W	**Status RAM Test Mode Enable** Set this bit to 1 to enable Status RAM Test mode, which will allow read/write access to the RX status FIFO. The address is specified in bit4-0 Status RAM address field. The data is written to or read from the RXCFG register.
4-0	R/W	**Status RAM address** Used as the address for the receiver status FIFO when accessed through RXCFG during RAM test mode.

Bus Master Read Cycle Test Mode Generation

When the BMTEN bit is set to 1, the TX buffer manager will generate bus master read cycles on command. Several of the TX operational register bit fields are redefined to facilitate control of this mode.

TXDP Read cycle starting address (dword aligned only).

TXCFG:DRTH Length of read cycle in bytes (1-335 bytes). The actual length value is derived as follows: length[8:0] = {DRTH[5], 0, DRTH[4], 0, 0, DRTH[3:0]}.

NOTE: TXCFG:MXDMA is still utilized while in this test mode to control the maximum DMA size. It is recommended that TXCFG:MXDMA be set to 0 so that the byte count in TXCFG:DRTH will control the DMA length.

CR:TXE Write a "1" to this bit will invoke the read cycle.

The sequence required to generate bus master read cycle is as follows:

Write a 1 to CR:TXR (not necessary if this mode is invoked immediately after reset)

Write a 1 to PTSCR:BMTEN

Write a Dword aligned starting address to the TXDP reg

WRITE A BYTE LENGTH TO THE TXCFG:DRTH

Write a 1 to the CR:TXE

All data read during this bus master cycle is discarded (bit bucket). Read cycles can be initiated repetitively without resetting TX between cycles. TXDP, and TXCFG data are retained between cycles.

Bus Master Write Cycle Test Mode Generation

When the BMTEN bit is set to 1, the RX buffer manager will generate bus master write cycles on command. Several of the RX operational register bit fields are redefined to facilitate control of this mode.

RXDP	Write cycle starting address (Dword aligned only).
RXCFG:DRTH	Length of write cycle in bytes (1-335 bytes). The actual length value is derived as follows: length[8:0] = {DRTH[5], 0, DRTH[4], 0, 0, DRTH[3:0]}. NOTE: RXCFG:MXDMA is still utilized while in this test mode to control the maximum DMA size. It is recommended that RXCFG:MXDMA be set to 0 so that the byte count in the RXCFG:DRTH bits will control the DMA length.
RXstatus[22:0]	Write cycle data (this data byte value is used for all byte lanes – see below for data pattern)
CR:RXE	Writing a "1" to this bit will invoke the write cycle

Data from the Receive status FIFO is used to provide the bus data for the write cycles. A location in the RX status FIFO must be written and read using RAM test mode to initialize the desired data pattern. The status data mapping used for each byte lane (little endian) during the generated write cycles is as follows:

byte 0 : status[7:0]

byte 1 : status[15:8]

byte 2 : {status[0], status[22:16]}

byte 3 : status[8:1]

The sequence required to generate bus master write cycle is as follows:

Write a 1 to CR:RXR (not necessary if this mode is invoked immediately after reset)

Write a 1 to PTSCR:SRTMEN and 00000 to PTSCR:SRAMADR[4:0]

Write desired data pattern to RXCFG (Note: Only bits 22-0 are used)

Read RXCFG

Write a 1 to PTSCR:BMTEN

Write a dword aligned starting address to the RXDP register

Write a byte length to the RXCFG:DRTH

Write a 1 to the CR:RXE

Write cycles can be initiated repetitively without resetting RX between cycles. RXDP, RX status, and RXCFG data are retained between cycles.

The sequence from step 1 to step 4 also describes the status RAM test mode procedure, as a example with address 00000. Similarly, Transmit and Receive RAM test mode can be achieved as follows:

1. Write a 1 to CR:TXR (not necessary if this mode is invoked immediately after reset)
2. Write a 1 to PTSCR:TRTMEN and the address to PTSCR:TRRAMADR[20:12]

3. Write desired data pattern to TXCFG

4. Read RXCFG

Register 10h Interrupt Status

Default Value: 03008000h

Access: Read Only

This register indicates the source of an interrupt when the INTA pin goes active. Enabling the corresponding bits in the Interrupt Mask Register (IMR) allows bits in this register to produce an interrupt. When an interrupt is active, one or more bits in this register are set to a "1". The Interrupt Status Register reflects all current pending interrupts, regardless of the state of the corresponding mask bit in the IMR. Reading the ISR clears all interrupts. Writing to the ISR has no effect.

BIT	ACCESS	DESCRIPTION
31-29		**Reserved**
28	RO	**Wake Up Event** Indicates that there is wake-up event occurs. This bit is a wired version of PM Event registers bits, it's not a registered one. So this bit will not be cleared by read operation like others status bits do, it is read as '0' when all PM Event registers bits are cleared.
27	RO	**End of Transmission Pause** Indicates pause command is completed when pause timer expires.
26	RO	**Start of Transmission Pause** Indicates data transmission is paused.
25	RO	**Transmit Reset Complete** Indicates that a requested transmit reset operation is complete.
24	RO	**Receive Reset Complete** Indicates that a requested receive reset operation is complete.
23	RO	**Detected Parity Error** This bit is set whenever CFGCS:DPERR is set, but cleared (like all other ISR bits) when the ISR register is read.
22	RO	**Signaled System Error** SiS900 signaled a system error on the PCI bus.
21	RO	**Received Master Abort** SiS900 received a master abort on the PCI bus.
20	RO	**Received Target Abort** SiS900 received a target abort on the PCI bus.
19-17		**Reserved**
16	RO	**RX Status FIFO Overrun** Set when an overrun condition occurs on the RX Status FIFO.

15	RO	**High Bits Error Set** A logical OR of bits 25-16
14-13		**Reserved**
12	RO	**Software Interrupt** Set whenever the SWI bit in the CR register is set.
11		**Reserved**
10	RO	**TX Underrun** Set when a transmit data FIFO underrun condition occurs.
9	RO	**TX Idle** This event is signaled when the transmit state machine enters the idle state from a non-idle state. This will happen whenever the state machine encounters an "end-of-list" condition (NULL link field or a descriptor with OWN clear).
8	RO	**TX Packet Error** This event is signaled after the last transmit descriptor in a failed transmission attempt that has been updated with valid status.
7	RO	**TX Descriptor** This event is signaled after a transmitter descriptor with the INTR bit set in the CMDSTS field that has been updated.
6	RO	**TX Packet OK** This event is signaled after the last transmit descriptor in a successful transmission attempt has been updated with valid status
5	RO	**RX Overrun** Set when a receive data FIFO overrun condition occurs.
4	RO	**RX Idle** This event is signaled when the receive state machine enters the idle state from a running state. This will happen whenever the state machine encounters an "end-of-list" condition (NULL link field or a descriptor with OWN set).
3	RO	**RX Early Threshold** Indicates that the initial RX Drain Threshold has been met by the incoming packet, and the transfer of the number of bytes specified by the DRTH field in the RXCFG register has been completed by the receive DMA engine. This interrupt condition will occur only once per packet.
2	RO	**RX Packet Error** This event is signaled after the last receive descriptor in a failed packet reception that has been updated with valid status.

1	RO	**RX Descriptor** This event is signaled after a receiver descriptor with the INTR bit set in the CMDSTS field that has been updated.
0	RO	**RX OK** Set by the receive state machine following the update of the last receive descriptor in a good packet.

Register 14h Interrupt Mask

Default Value: 00000000h

Access: Read/Write

This register masks the interrupts that can be generated from the ISR. Writing a "1" to the bit enables the corresponding interrupt. During hardware reset, all mask bits are cleared.

BIT	ACCESS	DESCRIPTION
31-29		**Reserved**
28	R/W	**Wake Up Event** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
27	R/W	**End of Transmission Pause** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
26	R/W	**Start of Transmission Pause** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
25	R/W	**Transmit Reset Complete** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
24	R/W	**Receive Reset Complete** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
23	R/W	**Detected Parity Error** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
22	R/W	**Signaled System Error** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
21	R/W	**Received Master Abort** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.

20	R/W	**Received Target Abort** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
19-17		**Reserved**
16	R/W	**RX Status FIFO Overrun** Set when an overrun condition occurs on the RX Status FIFO.
15	R/W	**High Bits Error Set** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
14-13		**Reserved**
12	R/W	**Software Interrupt** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
11		**Reserved**
10	R/W	**TX Underrun** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
9	R/W	**TX Idle** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
8	R/W	**TX Packet Error** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
7	R/W	**TX Descriptor** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
6	R/W	**TX Packet OK** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
5	R/W	**RX Overrun** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
4	R/W	**RX Idle** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
3	R/W	**RX Early Threshold** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.

2	R/W	**RX Packet Error** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
1	R/W	**RX Descriptor** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.
0	R/W	**RX OK** When this bit is 0, the corresponding bit in the ISR will not cause an interrupt.

The Interrupt Mask Register provides a mechanism for enabling individual interrupt sources in the Interrupt Status Register (ISR). Setting a mask bit allows the corresponding bit in the ISR to cause an interrupt. ISR bits are always set to 1, however, if the condition is present, regardless of the state of the corresponding mask bit.

Register 18h Interrupt Enable

Default Value: 00000000h

Access: Read/Write

The Interrupt Enable Register controls the hardware INTR signal.

BIT	ACCESS	DESCRIPTION
31-1		**Reserved**
0	R/W	**Interrupt Enable** When set to 1, the hardware INTR signal is enabled. When set to 0, the hardware INTR signal will be masked, and no interrupts will be generated. The setting of this bit has no effect on the ISR or IMR. This provides the ability to disable the hardware interrupt to the host with a single access (eliminating the need for a read-modify-write cycle).

Register 1Ch Enhanced PHY Access

Default Value: 00000000h

Access: Read/Write

SiS900 provides ten internal MII PHY registers for internal PHY configuration settings and status readings. Driver can access the ten internal MII registers by defining the command, Register offset, desired data from the ENPHY resister listed below.

BIT	ACCESS	DESCRIPTION
31-16	R/W	**R/W PHY Data** When write, this field specifies the data written to PHY register. When read, this field contains the data returned by PHY.
15-11		**Reserved**

10-6	R/W	**Register Address of PHY** Indicates the offset of PHY register.
5	R/W	**Access CMD to PHY** When '1', HW will issue a read operation to PHY registers, when '0', HW will issue a write operation. This field is valid only when bit 4 is '1'.
4	R/W	**SW Access Request/HW Done** When SW wants to access PHY register, it sets this bit to request HW. For such operation, HW will perform the access operation in a proper time, when finished, it clears this bit. SW can't change the PHY access contents if the current access is not done.
3-0		**Reserved**

Register 20h Transmit Descriptor Pointer

Default Value: 00000000h

Access: Read/Write

This register points to the current Transmit Descriptor.

BIT	ACCESS	DESCRIPTION
31-2	R/W	**Transmit Descriptor Pointer** The current value of transmitter descriptor pointer. When the transmit state machine is idle, software must set TXDP to the address of a completed transmit descriptor. While the transmit state machine is active, TXDP will follow the state machine as it advances through a linked list of active descriptors. If the link field of the current transmit descriptor is NULL (signifying the end of the list), TXDP will not advance, but will remain on the current descriptor. Any subsequent writes to the TXE bit of the CR register will cause the transmit state machine to reread the link field of the current descriptor to check for new descriptors that may have been appended to the end of the list. Transmit descriptors must be aligned on an even 32-bit boundary in host memory (A1-A0 must be 0).
1-0		**Reserved**

Register 24h Transmit Configuration

Default Value: 00800102h

Access: Read/Write

This register defines the Transmit Configuration for SiS900. It controls such functions as Loopback, Auto Transmit Padding, Fill & Drain Thresholds, and maximum DMA burst size.

BIT	ACCESS	DESCRIPTION

31	R/W	**Carrier Sense Ignore** Setting this bit to 1 causes the transmitter to ignore carrier sense activity, which inhibits reporting of CRS status to the transmitter status register. When this bit is 0 (default), the transmitter will monitor the CRS signal during transmission and reflect valid status in the transmitter status register. This bit must be set to enable full-duplex operation.
30	R/W	**HeartBeat Ignore** Setting this bit to 1 causes the transmitter to ignore the heartbeat (CD) pulse that follows the packet transmission. When this bit is set to 0 (default), the transmitter will monitor the heartbeat pulse. This bit must be set to enable full-duplex operation
29	R/W	**MAC Loopback** Setting this bit to a 1 places SiS900 into a controller loopback state which routes all transmit traffic to the receiver, and disables the transmit and receive interfaces of the MII. A 0 in this bit allows normal MAC operation. The transmitter and receiver must be disabled before enabling the loopback mode. (Packets received during MLB mode will reflect loopback status in the receive descriptor‘s CMDSTS.LBP field.)
28	R/W	**Automatic Transmit Padding** Setting this bit to 1 causes the MAC to automatically pad small (runt) transmit packets to the Ethernet minimum size of 64 bytes. This allows driver software to transfer only actual packet data. Setting this bit to 0 disables the automatic padding function, forcing software to control runt padding.
27-25		**Reserved**
24-23		Writes are ignored, reads return 01.
22-20	R/W	**Max DMA Burst Size per TX DMA Burst** This field sets the maximum size of transmit DMA data bursts according to the following table: 000 128 x 32-bit words (512 bytes) 001 1 x 32-bit word (4 bytes) 010 2 x 32-bit words (8 bytes) 011 4 x 32-bit words (16 bytes) 100 8 x 32-bit words (32 bytes) 101 16 x 32-bit words (64 bytes) 110 32 x 32-bit words (128 bytes) 111 64 x 32-bit words (256 bytes)
19-14		**Reserved**

13-8	R/W	**TX Fill Threshold** Specifies the fill threshold in units of 32 bytes. When the number of available bytes in the transmitter FIFO reaches this level, the transmit bus master state machine will be allowed to request the PCI bus for transmit packet fragment reads. A value of 0 in this field will produce unexpected results and must not be used.
7-6		**Reserved**
5-0	R/W	**TX Drain Threshold** Specifies the drain threshold in units of 32 bytes. When the number of bytes in the FIFO reaches this level (or the FIFO contains at least one complete packet) the MAC transmit state machine will begin the transmission of a packet. NOTE: In order to prevent a deadlock condition from occurring, the transmit drain threshold should never be set higher than the (TXFIFOSize – TXCFG:FLTH). A value of 0 in this field will produce unexpected results and must not be used.

Register 30h This register points to the current Receive Descriptor.

Default Value: 00000000h

Access: Read/Write

This register points to the current Receive Descriptor.

BIT	ACCESS	DESCRIPTION
31-2	R/W	**Receive Descriptor Pointer** The current value of the receiver descriptor pointer. When the receive state machine is idle, software must set RXDP to the address of an available receive descriptor. While the receive state machine is active, RXDP will follow the state machine as it advances through a linked list of available descriptors. If the link field of the current receive descriptor is NULL (signifying the end of the list), RXDP will not advance, but will remain on the current descriptor. Any subsequent writes to the RXE bit of the CR register will cause the receive state machine to reread the link field of the current descriptor to check for new descriptors that may have been appended to the end of the list. Software should not write to this register unless the receive state machine is idle. Receive descriptors must be aligned on 32-bit boundaries (A1-A0 must be zero).
1-0		**Reserved**

Register 34h Receive Configuration

Default Value: 00000002h

Access: Read/Write

This register is used to set the receiver configuration for SiS900. Receive properties such as

accepting error packets, runt packets, setting the receive drain threshold etc. are controlled here.

BIT	ACCESS	DESCRIPTION
31	R/W	**Accept Errors Packets** When set to 1, all packets with CRC, alignment, and/or collision errors will be accepted. When set to 0, all packets with CRC, alignment, and/or collision errors will be rejected if possible. Note that depending on the type of error, some packets may be received with errors, regardless of the setting of AEP. These errors will be indicated in the CMDSTS field of the last descriptor in the packet.
30	R/W	**Accept Runt Packets** When set to 1, all packets under 64 bytes in length without errors are accepted. When this bit is 0, all packets less than 64 bytes in length will be rejected if possible.
29		**Reserved**
28	R/W	**Accept Transmit Packets** When set to 1, data received simultaneously to a local transmission (such as during a PMD loopback or full duplex operation) will be accepted as valid received data. Additionally, when set to 1, the receiver will ignore collision activity. When set to 0 (default), all data receive simultaneous to a local transmit will be rejected. This bit must be set to 1 for PMD loopback and full duplex operation.
27	R/W	**Accept Jabber Packets** When set to 1, all packets over 1518 bytes in length (to a maximum of 2046 bytes) will be accepted and placed in the receive data buffers (if buffers that large are specified in the receive descriptor list). When set to 0, packets larger than 1518 bytes (CRC inclusive) will be rejected if possible. A byte count of 2046 indicates that the packet may have been truncated.
26-23		**Reserved**
22-20	R/W	**Max DMA Burst Size per RX DMA Burst** This field sets the maximum size of receive DMA data bursts according to the following table: 000 128 x 32-bit words (512 bytes) 001 1 x 32-bit word (4 bytes) 010 2 x 32-bit words (8 bytes) 011 4 x 32-bit words (16 bytes) 100 8 x 32-bit words (32 bytes) 101 16 x 32-bit words (64 bytes) 110 32 x 32-bit words (128 bytes) 111 64 x 32-bit words (256 bytes)
19-6		**Reserved**

5-1	R/W	**RX Drain Threshold** Specifies the drain threshold in units of 8 bytes. When the number of bytes in the receiver FIFO reaches this value (times 8), or the FIFO contains a complete packet, the receive bus master state machine will begin the transfer of data from the FIFO to host memory. Care must be taken when setting DRTH to a value lower than the number of bytes needed to determine if packet should be accepted or rejected. In this case, the packet might be rejected after the bus master operation to begin transferring the packet into memory has begun. When this occurs, neither the OK bit nor any error status bit in the descriptor's CMDSTS will be set. A value of 0 is illegal, and the results are undefined. This value is also used to compare with the accumulated packet length for early receive indication. When the accumulated packet length meets or exceeds the DRTH value, the RXEARLY interrupt condition is generated.
0		**Reserved**

Register 38h Flow Control

Default Value: 00000000h

Access: Read/Write

The FLOWCTL register is used to control and configure SiS900 Flow Control logic. The Flow Control Logic is used to detect PAUSE frame packets and control data frame transmission.

BIT	ACCESS	DESCRIPTION
31-2		**Reserved**
1	R/W	**PAUSE Flag** When "1" indicates data frame transmission is paused. When "0" transmission is normal. This bit is reset by H/W reset, 900 soft reset, transmit reset, pause timer expires or S/W write 0 to this bit.
0	R/W	**Flow Control Enable** Set to 1, enable the PAUSE frame detection. Set to 0, disable the PAUSE frame detection. This bit is reset only by H/W reset.

Register 48h Receive Filter Control

Default Value: 00000000h

Access: Read/Write

The RFCR register is used to control and configure SiS900 Receive Filter Control logic. The Receive Filter Control Logic is used to configure destination address filtering of incoming packets.

BIT	ACCESS	DESCRIPTION

31	R/W	**RX Filter Enable** When this bit is set to 1, the RX Filter is enabled to qualify incoming packets. When set to 0, receive packet filtering is disabled (i.e. all receive packets are rejected).
30	R/W	**Accept All Broadcast** When set to 1, this bit causes all broadcast address packets to be accepted. When set to 0, no broadcast address packets will be accepted.
29	R/W	**Accept All Multicast** When set to 1, this bit causes all multicast address packets to be accepted. When set to 0, multicast destination addresses must have the appropriate bit set in the multicast hash table mask in order for the packet to be accepted.
28	R/W	**Accept All Physical** When set to 1, this bit causes all physical address packets to be accepted. When set to 0, the destination address must match the node address register in order for the packet to be accepted.
27-20		**Reserved**
19-16	R/W	**Receive Filter Address** Selects which internal receive filter register is accessible via RFDR: 0000 node address octets 1-0 0001 node address octets 3-2 0010 node address octets 5-4 0011 RESERVED 0100 multicast hash table bits 15-0 0101 multicast hash table bits 31-16 0110 multicast hash table bits 47-32 0111 multicast hash table bits 63-48 1000 multicast hash table bits 79-64 1001 multicast hash table bits 95-80 1010 multicast hash table bits 111-96 1011 multicast hash table bits 127-112 others RESERVED
15-0		**Reserved**

Register 4Ch Receive Filter Data

Default Value: 00000000h

Access: Read/Write

The RFDR register is used for reading from and writing to the internal receive filter registers (unique address register, and the hash table register).

BIT	ACCESS	DESCRIPTION
31-16		**Reserved**

15-0	R/W	**Receiver Filter Data** Receiver Filter Data

The Receive Filter Logic uses the following algorithm when qualifying incoming packets for reception:

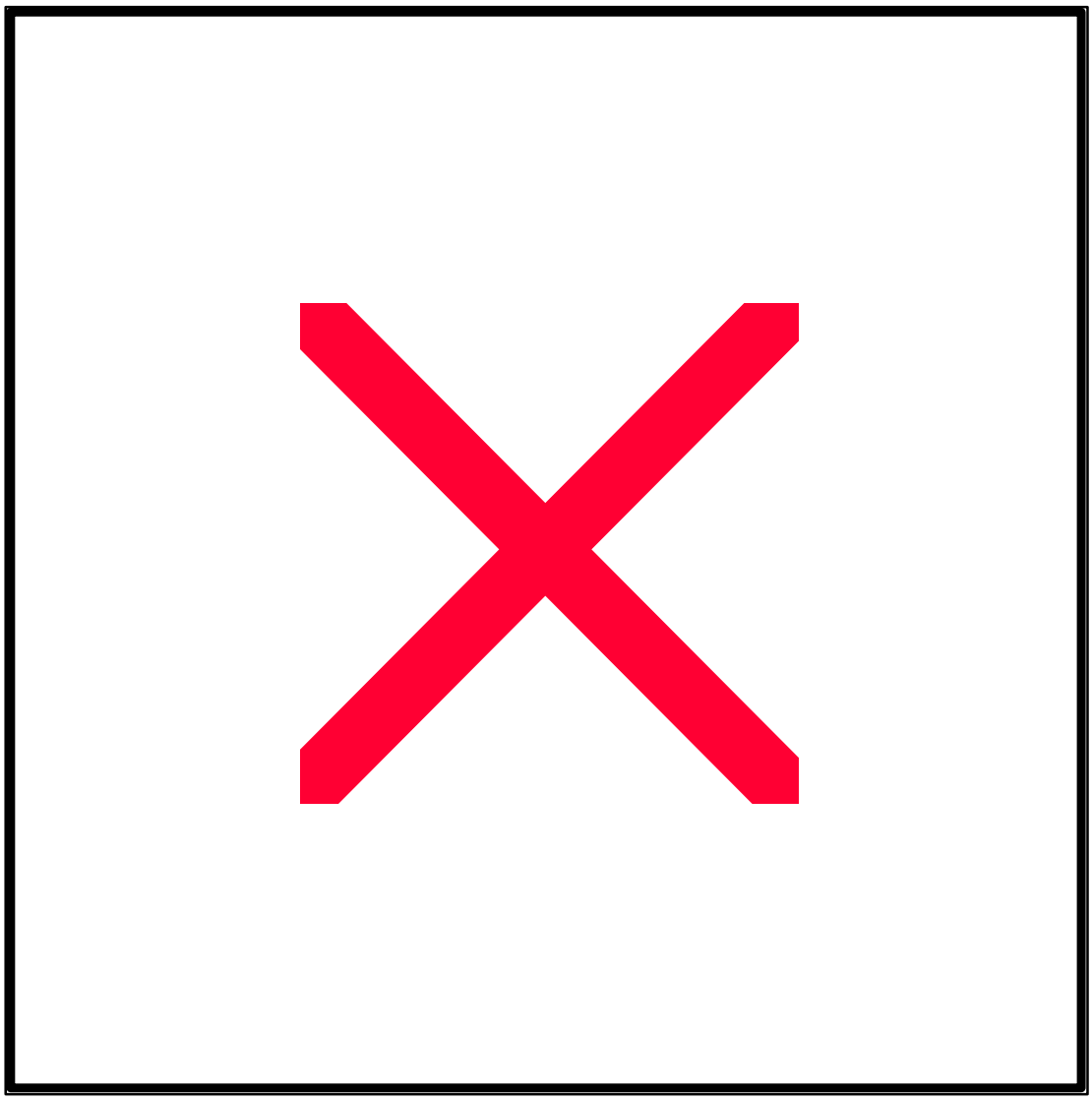
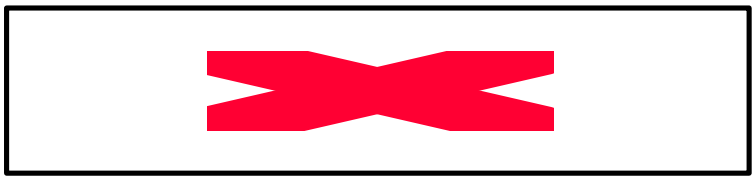


Figure 8.7-1 Receive Filter Algorithm

The *Node Address* register is a 48-bit register internal to the Receive Filter logic. When RFCR:AAP is clear, then the receive filter logic will only accept unicast packets which match the contents of the node address register. Octet 0 of the node address register corresponds to the first octet of the packet as it appears on the wire. Octet 5 of the node address register corresponds to the last octet of the destination address as it appears on the wire. For example, to configure a node address of 00-E0-06-07-28-55,

Software would need to execute the following series of register operations:



```
out32( RFCR, 0x00000000 );     /* disable receive filter, NA(0) */
out32( RFDR, 0x0000E000 );     /* load octets 0 and 1 */
out32( RFCR, 0x00010000 );     /* select NA[1] */
out32( RFDR, 0x00000706 );     /* load octets 2 and 3 */
out32( RFCR, 0x00020000 );     /* select NA[2] */
out32( RFDR, 0x00005528 );     /* load octets 4 and 5 */
out32( RFCR, 0xC0000000 );     /* enable receive filter, accept broadcasts */
```

The *Multicast Hash Table* register can be configured to perform imperfect filtering of multicast packets. If the receive packet's destination address is a multicast address (but not the broadcast address) and the RFCR:AAM is not set, then the receive filter logic will use the 7 most significant bits of the destination address's CRC as an index into the Multicast Hash Table register. If the corresponding bit is set, then the packet is accepted, otherwise the packet is rejected. Refer to Appendix B - Hash Table Index Computation.

Register B0h Power Management Control

Default Value: 00000000h

Access: Read/Write

This register provides SW an interface to control which Power Management Event to assert PME# / INTA#. The contents of this register should be well-programmed before set the Ethernet Controller into power saving state, and will not be affected by PCI HW reset. It can be reset by software reset (OP register offset 00h bit8) except ISOSEL.

BIT	ACCESS	DESCRIPTION
31	R/W	**Gate Dual Target Clock Enable** When '1', the clock of dual powered blocks will be gated when in (D3cold and (not PME_EN)). When '0', the clock of dual powered blocks will never be gated.
30	R/W	**Wake-up While Receive OK Packet** When '1', any packet that passed the RXFilter with no error will cause a wake-up event. This may include any broadcast, multicast, or direct addressed packet depending on how RXFilter is programmed.
29-27		**Reserved**

26	R/W	**3rd Wake-up Frame Access** When '1', access to WAKECRC is indirectly mapped to the 3rd wake-up frame CRC register. FRM3ACS, FRM2ACS, and FRM1ACS are supposed not to be set at the same time for read access.
25	R/W	**2nd Wake-up Frame Access** When '1', access to WAKECRC is indirectly mapped to the 2nd wake-up frame CRC register. FRM3ACS, FRM2ACS, and FRM1ACS are supposed not to be set at the same time for read access.
24	R/W	**1st Wake-up Frame Access** When '1', access to WAKECRC is indirectly mapped to the 1st wake-up frame CRC register. FRM3ACS, FRM2ACS, and FRM1ACS are supposed not to be set at the same time for read access.
23		**Reserved**
22	R/W	**3rd Wake-up Frame Match Enable** When this bit is '1', and PME_EN is '1', the 3rd wake-up mechanism of receipt of a network wake-up frame is enabled.
21	R/W	**2nd Wake-up Frame Match Enable** When this bit is '1', and PME_EN is '1', the 2nd wake-up mechanism of receipt of a network wake-up frame is enabled.
20	R/W	**1st Wake-up Frame Match Enable** When this bit is '1', and PME_EN is '1', the 1st wake-up mechanism of receipt of a network wake-up frame is enabled.
19-12		**Reserved**
11	R/W	**Magic PacketTM Match Algorithm** When '1', a strict magic packet match algorithm is used when detect magic packet. When '0', a loose magic packet match algorithm is used when detects magic packet.
10	R/W	**Magic PacketTM Match Enable** When this bit is '1', and PME_EN is '1', the wake-up mechanism of receipt of a Magic Packet is enabled.
9-2		**Reserved**
1	R/W	**Link On Monitor Enable** When this bit is '1', and PME_EN is '1', the wake-up mechanism of detection the link on state is enabled.
0	R/W	**Link Loss Monitor Enable** When this bit is '1', and PME_EN is '1', the wake-up mechanism of detection the link loss state is enabled.

Register B4h Power Management Wake-up Event

Default Value: 00000000h

Access: Read/Write

This register records which wake-up event wake up the system. This register is not affected by PCI HW reset. It can be reset only by software reset (OP register offset 00h bit8). SW writes 1 will clear the individual bits. SW writes 0 will leave the individual bits unchanged.

BIT	ACCESS	DESCRIPTION
31		**Reserved**
30	R/W	**Receive OK Packet** H/W sets this bit whenever bit30 of PM Control Register is '1' and an incoming packet passes the RXFilter with no error. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
29-23		**Reserved**
22	R/W	**Match 3rd Wake-up Sample Frame** H/W sets this bit whenever bit22 of PM Control Register is '1' and receipt of the pre-defined 3rd wake-up frame with no error. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
21	R/W	**Match 2nd Wake-up Sample Frame** H/W sets this bit whenever bit21 of PM Control Register is '1' and receipt of the pre-defined 2nd wake-up frame with no error. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
20	R/W	**Match 1st Wake-up Sample Frame** H/W sets this bit whenever bit20 of PM Control Register is '1' and receipt of the pre-defined 1st wake-up frame with no error. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
19-11		**Reserved**
10	R/W	Magic Packet™ Match H/W sets this bit whenever bit10 of PM Control Register is '1' and receipt of a magic packet with no error. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.
9-2		**Reserved**
1	R/W	**Link On Event** H/W sets this bit whenever bit1 of PM Control Register is '1' and link status changes from loss to on. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.

0	R/W	**Link Loss Event** H/W sets this bit whenever bit0 of PM Control Register is '1' and link status changes from on to loss. SW writes '1' to this bit will clear this bit. SW writes '0' to this bit leaves this bit unchanged.

Register BCh Wake-up Sample Frame CRC

Default Value: 00000000h

Access: Read/Write

This register provides an access window to the CRC values of the mask bytes in wake-up sample frames. When FRM3ACS, FRM2ACS, or FRM1ACS is '1', the CRC value of the mask bytes in the corresponding wake-up sample frame can be accessed through this register. FRM3ACS, FRM2ACS, and FRM1ACS are supposed not to be set at the same time for read access. If the CRC value of those incoming bytes, whose byte mask is set to 1 in the sample frame, equals to the CRC value in the sample frame, then the incoming frame is considered a wake-up frame. This register is not affected by PCI HW reset. It can be reset only by software reset (OP register offset 00h bit8).

BIT	ACCESS	DESCRIPTION
31-0	R/W	**Wake-up Frame CRC Value** This field specifies the CRC value of the mask bytes in the corresponding wake-up sample frame specified by FRM3ACS, FRM2ACS, and FRM1ACS. H/W uses this 32-bit CRC value to match the 32-bit CRC value of incoming frame mask bytes. If matched, the incoming frame is a wake-up frame and PME# will be asserted if enabled.

8.7.1 WAKE-UP SAMPLE FRAME BYTE MASK REGISTER

These registers provide the mask bytes in wake-up sample frames. These registers are not affected by PCI HW reset. They can be reset by software reset (OP register offset 00h bit8).

REGISTER	SIZE	R/W	DESCRIPTION
C0h	32	R/W	The 1st 32 byte mask in the 1st Wake-up sample frame.
C4h	32	R/W	The 2nd 32 byte mask in the 1st Wake-up sample frame.
C8h	32	R/W	The 3rd 32 byte mask in the 1st Wake-up sample frame.
CCh	32	R/W	The 4th 32 byte mask in the 1st Wake-up sample frame.
D0h	32	R/W	The 1st 32 byte mask in the 2nd Wake-up sample frame.
D4h	32	R/W	The 2nd 32 byte mask in the 2nd Wake-up sample frame.
D8h	32	R/W	The 3rd 32 byte mask in the 2nd Wake-up sample frame.
DCh	32	R/W	The 4th 32 byte mask in the 2nd Wake-up sample frame.
E0h	32	R/W	The 1st 32 byte mask in the 3rd Wake-up sample frame.
E4h	32	R/W	The 2nd 32 byte mask in the 3rd Wake-up sample frame.

E8h	32	R/W	The 3rd 32 byte mask in the 3rd Wake-up sample frame.
ECh	32	R/W	The 4th 32 byte mask in the 3rd Wake-up sample frame.

8.8 MII PHY REGISTERS

8.9 MII PHY REGISTERS

SiS960 has eleven internal MII PHY 16 bit registers. Ten registers are available for setting configuration inputs and reading status outputs and one register is reserved for factory use. The ten accessible registers consist of six registers that are defined by IEEE 802.3 specification (MI Register 0-5) and four registers that are unique to SiS960 (MI Register 16-19).

The accesses of the ten MI PHY Registers are through MAC Operational Register ENPHY (offset 1Ch). Users can define the command (RWCMD, ENPHY bit 5), the Register Offset (REGADDR, ENPHY bit 10-6), and the Data contents (PHYDATA, ENPHY bit 31-16). And then the driver issue the access command bit by writing '1' to register ENPHY bit 4, ACCESS, and wait for SiS960 complete the operation which should return '0' when completed.

Table 4-3 PHY Configuration Register Map

REGISTER	TAG	DESCRIPTION	ACCESS	SECTION
00h	CONTROL	MI Register 0 Control Register	RO	4.4.1
01h	STATUS	MI Register 1 Status Register	R/W	4.4.2
02h	PHYID1	MI Register 2 PHY ID#1	RO	4.4.3
03h	PHYID2	MI Register 3 PHY ID#2	R/W	4.4.4
04h	AUTOADV	MI Register 4 Auto Negotiation Advertisement	R/W	4.4.5
05h	AUTOREC	MI Register 5 Auto Negotiation Remote End Capability	R/W	4.4.6
10h	CONFIG1	MI Register 16 Configuration 1	R/W	4.4.7
11h	CONFIG2	MI Register 17 Configuration 2	R/W	4.4.8
12h	STSOUT	MI Register 18 Status Output	R/LT	4.4.9
13h	MASK	MI Register 19 Mask	R/W	4.4.10
14h	RESERVED	MI Register 20 Reserved	R/W	4.4.11

Register 00h CONTROL

Default Value: 3000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION

15	R/WSC	**PHY Reset** 1 Reset, Bit Self Cleaning After Reset Completed 0 Normal
14	R/W	**Loopback** 1 Loopback Mode Enabled 0 Normal
13	R/W	**Speed** 1 100 Mbps Selected (100Base TX) 0 10 Mbps selected (10Base-T)
12	R/W	**Auto-Negotiation** 1 Auto-Negotiation Enabled 0 Normal
11	R/W	**Powerdown** 1 Powerdown 0 Normal
10	R/W	**MII interface** 1 MII Interface Disabled 0 Normal
9	R/WSC	**Auto-Negotiation Reset** 1 Reset Auto-Negotiation Process, Bit Self Clearing After Reset Completed 0 Normal
8	R/W	**Duplex Mode** 1 Full Duplex 0 Half Duplex
7	R/W	**Collision Test** 1 Collision Test Enabled 0 Normal
6-0	R/W	**Reserved**

Register 01h STATUS

Default Value: 7809h

Access: Read Only

BIT	ACCESS	DESCRIPTION
15	RO	0 Not Capable of 100Base-T4 Operation
14	RO	1 Capable of 100Base-TX Full Duplex
13	RO	1 Capable of 100Base-TX Half Duplex
12	RO	1 Capable of 10Base-T Full Duplex
11	RO	1 Capable of 10Base-T Half Duplex
10-7	RO	Reserved

6	R	0 Not Capable of Accepting MI Frames with MI Preamble Suppressed
5	R	1 Auto-Negotiation Acknowledge Process Complete 0 Normal
4	R/LH	1 Remote Fault Detected. This bit is set when Either Interrupt Detect or Auto-Negotiation Remote Fault is set. 0 No Remote Fault
3	R	1 Capable of Auto-Negotiation Operation
2	R/LL	1 Link Detected 0 Link not detected
1	R/LH	1 Jabber Detected 0 Normal
0	R	1 Extended Register Exist

Register 02h PHY ID #1

Default Value: 001Dh

Access: Read

BIT	ACCESS	DESCRIPTION
15-0	R	**Company ID, Bits 3-18** OUI = 00-E0-06

Register 03h PHY ID #2

Default Value: 8000h

Access: Read

BIT	ACCESS	DESCRIPTION
15-10	R	**Company ID, Bits 19-24** OUI = 00-E0-06
9-4	R	**Manufacturer's Part Number** 00_H
3-0	R	**Manufacturer's Revision Number** 00_H

Register 04h Auto-Negotiation Advertisement

Default Value: 05E1h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15	R/W	1 Next Page Exists 0 No Next Page

14	R	1 Received Auto-Negotiation Word Recognized 0 Not Recognized
13	R/W	1 Auto-Negotiation Remote Fault Detected 0 No Remote Fault
12-11	R/W	RESERVED
10	R/W	1 Capable of Pause Operation for Full Duplex Link 0 Not Capable
9	R/W	1 Capable of 100Base-T4 0 Not Capable
8	R/W	1 Capable of 100Base-TX Full Duplex 0 Not Capable
7	R/W	1 Capable of 100Base-TX Half Duplex 0 Not Capable
6	R/W	1 Capable of 10Base-T Full Duplex 0 Not Capable
5	R/W	1 Capable of 10Base-T Half Duplex 0 Not Capable
4-1	R/W	RESERVED
0	R/W	1 Capable of 802.3 CSMA Operation 0 Not Capable

Note 1: Next Page currently not supported.

Register 05h Auto-Negotiation Remote End Capability

Default Value: 0000h

Access: Read

BIT	ACCESS	DESCRIPTION
15	R	1 Next Page Exists 0 No Next Page
14	R	1 Received Auto-Negotiation Word Recognized 0 Not Recognized
13	R	1 Auto-Negotiation Remote Fault Detected 0 No Remote Fault
12-11	R	Reserved
10	R	1 Capable of Pause Operation for Full Duplex Link 0 Not Capable
9	R	1 Capable of 100Base-T4 0 Not Capable
8	R	1 Capable of 100Base-TX Full Duplex 0 Not Capable

7	R	1 Capable of 100Base-TX Half Duplex 0 Not Capable
6	R	1 Capable of 10Base-T Full Duplex 0 Not Capable
5	R	1 Capable of 10Base-T Half Duplex 0 Not Capable
4-1	R	RESERVED
0	R	1 Capable of 802.3 CSMA Operation 0 Not Capable

Register 10h Configuration 1

Default Value: 0022h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15	R/W	**Link Disable** 1 Received Link Detect Function Disabled (Force Link Pass) 0 Normal
14	R/W	**Transmit Disable** 1 TP Transmitter Disabled 0 Normal
13	R/W	**Transmit Powerdown** 1 TP Transmitter Powered Down 0 Normal
12	R/W	**TX_EN to CRS Loopback** 1 TX_EN to CRS Loopback Disabled 0 Enabled
11-10	R/W	RESERVED
9	R/W	**Unscrambled Idle Reception Disable** 1 Disable Auto-Negotiation with devices that transmit unscrambled, idle on power up and various instances 0 Enables Auto-Negotiation with devices that transmit unscrambled, idle on power up and various instances
8	R/W	**Receive Equalizer Select** 1 Received Equalizer Disabled, Set to 0 Length 0 Receive Equalizer On (For 100Base-TX Mode Only)
7	R/W	**Cable Type Select** 1 STP (150 Ohm) 0 UTP (100 Ohm)
6	R/W	**Receive Input Level Adjust** 1 Receive Squelch Levels Reduced By 4.5 dB 0 Normal

5-2	R/W	Reserved
1-0	R/W	**Transmitter Rise/Fall Time Adjust** 11 -0.25 ns 10 +0.0 ns 01 +0.25 ns 00 +0.5 ns

Register 11h Configuration 2

Default Value: FF00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15-6	R	**Reserved**
5	R/W	**Auto Polarity Disable** 1 Auto Polarity Correction Function Disabled 0 Normal
4	R/W	**Jabber Disable Select** 1 Jabber Disabled 0 Enabled
3-0	R/W	**Reserved**

Register 12h Status Output REGISTER

Default Value: 0080h

Access: Read Only

BIT	ACCESS	DESCRIPTION
15	RO	**Interrupt Detec**t 1 Interrupt Bit(s) Have Changed Since Last Read Operation. 0 No Change
14	R/LT	**Link Fail Detect** 1 Link Not Detected 0 Normal
13	R/LT	**Descrambler Loss of Synchronization Detect** 1 Descrambler Has Lost Synchronization 0 Normal
12	R/LT	**Codeword Error** 1 Invalid 4B/5B Code Detected On Receive Data 0 Normal
11	R/LT	**Start Of Stream Error** 1 No Start Of Stream Delimiter Detected on Received Data 0 Normal

10	R/LT	**End Of Stream Error** 1 No End Of Stream Delimiter Detected On Receive Data 0 Normal
9	R/LT	**Reverse Polarity Detect** 1 Reserve Polarity Detected 0 Normal
8	R/LT	**Jabber Detect** 1 Jabber Detected 0 Normal
7	R/LT	**100/10 Speed Detect** 1 Device in 100 Mbps Mode (100Base-TX) 0 Device in 10 Mbps Mode (10Base-T)
6	R/LT	**Duplex Detect** 1 Device In Full Duplex 0 Device In Half Duplex
5-4	RO	**Auto-Negotiation Status** 11 Auto-Negotiation Detected & Started 10 Auto-Negotiation Detected & Stuck 01 Auto-Negotiation Detected & Done 00 Auto-Negotiation Not Detected
3-0	RO	**Reserved**

Register 13h Mask

Default Value: FFC0h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15	R/W	1 Mask Interrupt For INT in Register 18 0 No Mask
14	R/W	1 Mask Interrupt For LNK_FAIL in Register 18 0 No Mask
13	R/W	1 Mask Interrupt For LOSS_SYNC in Register 18 0 No Mask
12	R/W	1 Mask Interrupt For CWRD in Register 18 0 No Mask
11	R/W	1 Mask Interrupt For SSD in Register 18 0 No Mask
10	R/W	1 Mask Interrupt For ESD in Register 18 0 No Mask
9	R/W	1 Mask Interrupt For RPOL in Register 18 0 No Mask
8	R/W	1 Mask Interrupt For JAB in Register 18 0 No Mask

7	R/W	1 Mask Interrupt For SPD_DET in Register 18 0 No Mask
6	R/W	1 Mask Interrupt For DPLX_DET in Register 18 0 No Mask
5-3	R/W	**Reserved**
2-0	R/W	**Link Fail Timer Select** 111 Reserved 110 Bit 18.14 Set to 1 if Link Fail for >32 Sec 101 Bit 18.14 Set to 1 if Link Fail for >16 Sec 100 Bit 18.14 Set to 1 if Link Fail for >8 Sec 011 Bit 18.14 Set to 1 if Link Fail for >4 Sec 010 Bit 18.14 Set to 1 if Link Fail for >2 Sec 001 Bit 18.14 Set to 1 if Link Fail for >1 Sec 000 Bit 18.14 Set to 1 if Link Fail for >0 Sec

Register 14h RESERVED

Default Value: 0000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15-0	R/W	Reserved for Factory Use. Must to 0 for Normal Operation

8.10 USB OPENHCI HOST CONTROLLER CONFIGURATION SPACE

The base address of these registers is programmable by the memory base address register (USB PCI configuration register offset 10-13h). These registers should be written as Dword, byte writes to these registers have unpredictable effects.

The OpenHCI Host Controller (HC) contains a set of on-chip operational registers which are mapped into a non-cacheable portion of the system addressable space. These registers are used by the Host Controller Driver (HCD). According to the function of these registers, they are divided into four partitions, specifically for Control and Status, Memory Pointer, Frame Counter and Root Hub. All of the registers should be read and written as Dwords.

Reserved bits may be allocated in future releases of this specification. To ensure interoperability, the Host Controller Driver that does not use a reserved field should not assume that the reserved field contains 0. Furthermore, the Host Controller Driver should always preserve the value(s) of the reserved field. When a R/W register is modified, the Host Controller Driver should first read the register, modify the bits desired, then write the register with the reserved bits still containing the read value. Alternatively, the Host Controller Driver can maintain an in-memory copy of previously written values that can be modified and then written to the Host Controller register. When a write to set/clear register is written, bits written to reserved fields should be 0.

8.10.1 CONTROL AND STATUS PARTITION

Register 00h HcRevision Register

Default Value: 00000110h

Access: Read

BIT	ACCESS	DESCRIPTION
31:9		**Reserved**
8	RO	**Legacy** This read-only field is 1 to indicate that the legacy support registers are present in this HC.
7:0	RO	**Revision** This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of 11h corresponds to version 1.1. All of the HC implementations that are compliant with current OpenHCI 1.0 specification will have a value of 10h.

Register 04h HcControl Register

Default Value: 00000000h

Access: Read/Write

The HcControl register defines the operating modes for the Host Controller. Only the Host Controller Driver, except Host Controller Functional State and Remote Wakeup Connected modifies most of the fields in this register.

BIT	ACCESS	DESCRIPTION
31:11		**Reserved**
10	R/O	**RemoteWakeupEnable** This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the Resume Detected bit in Hc Interrupt Status is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt. Since there is no remote wakeup supported, this bit is ignored.
9	RO	**Remote Wakeup Connected** This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system it is the responsibility of system firmware to set this bit during POST. HC clears the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification. This bit is hard-coded to '0'.

8	R/W	**Interrupt Routing** This bit determines the routing of interrupts generated by events registered in Hc Interrupt Status. If clear, all interrupts are routed to the normal host bus interrupt mechanism. If set, interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.
7:6	R/W	**HostControllerFunctionalState for USB** 00b: UsbReset 01b: UsbResume 10b: UsbOperational 11b: UsbSuspend A transition to UsbOperational from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartofFrame field of HcInterruptStatus. This field may be changed by HC only in the UsbSuspend state. HC may move from the UsbSuspend state to the UsbResume state after detecting the resume signal from a downstream port. HC enters UsbSuspend after a software reset, whereas it enters UsbReset after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signal to downstream ports.
5	R/W	**BulkListEnable** This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcBulkCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcBulkCurrentED before re-enabling the processing of the list.
4	R/W	**ControlListEnable** This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, the processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcControlCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcControlCurrentED before re-enabling the processing of the list.

3	R/W	**IsochronousEnable** This bit is used by HCD to enable/disable the processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).
2	R/W	**PeriodicListEnable** This bit is set to enable the processing of the periodic list in the next Frame. If cleared by HCD, the processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.
1:0	R/W	**ControlBulkServiceRatio** This specifies the service ratio between Control and Bulk EDs. Before processing any of the non-periodic lists, HC must compare the ratio specified with its internal count on how many non-empty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value. **CBSR** — **No. of Control EDs Over Bulk EDs Served** 0 — 1:1 1 — 2:1 2 — 3:1 3 — 4:1

Register 08h HcCommandStatus Register

Default Value: 00000000h

Access: Read/Write

The HcCommandStatus register is used by the Host Controller to receive commands issued by the Host Controller Driver, as well as reflects*** the current status of the Host Controller. To the Host Controller Driver, it appears to be a "write to set" register. The Host Controller must ensure those bits written as '1' become set in the register while those bits written as '0' remain unchanged in the register. The Host Controller Driver may issue multiple distinct commands to the Host Controller without concern for corrupting previously issued commands. The Host Controller Driver has normal read access to all bits.

The **SchedulingOverrunCount** field indicates the number of frames with which the Host Controller has detected the scheduling overrun error. This occurs when the Periodic list does not complete before EOF. When a scheduling overrun error is detected, the Host

Controller increments the counter and sets the **SchedulingOverrun** field in the HcInterruptStatus register.

BIT	ACCESS	DESCRIPTION
31:18		**Reserved**
17:16	RO	**SchedulingOverrunCount** These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if Scheduling Overrun in Hc Interrupt Status has already been set. This is used by HCD to monitor any persistent scheduling problems.
15:4		**Reserved**
3	R/W	**OwnershipChangeRequest** This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the Ownership Change field in HcInterrupt Status. After the changeover, this bit is cleared and remains so until the next request from OS HCD.
2	R/W	**BulkListFilled** This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set BulkListFilled to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.

1	R/W	**ControlListFilled** This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set ControlListFilled to 0. If HC finds a TD on the list, then HC will set ControlListFilled to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop
0	R/W	**HostControllerReset** This bit is set by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the UsbSuspend state in which most of the operational registers are reset except those stated otherwise; e.g., the InterruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 µs. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signal should be asserted to its downstream ports.

Register 0Ch *HcInterruptStatus* Register

Default Value: 00000000h

Access: Read/Write

This register provides status on various events that cause hardware interrupts. When an event occurs, Host Controller sets the corresponding bit in this register. When a bit is set, a hardware interrupt is generated if the interrupt is enabled in the *HcInterruptEnable* register and the **MasterInterruptEnable** bit is set. The Host Controller Driver may clear specific bits in this register by writing '1'to bit positions to be cleared. The Host Controller Driver may not set any of these bits. The Host Controller will never clear the bit.

BIT	ACCESS	DESCRIPTION
31		**Reserved**
30	R/W	**Ownership Change Status** This bit is set by HC when HCD sets the Ownership Change Request field in HcCommandStatus. This event, when unmasked, will always generate an System Management Interrupt (SMI#) immediately.
29:7		**Reserved**

6	R/W	**RootHubStatusChange Status** This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus[NumberofDownstreamPort] has changed.
5	R/W	**FrameNumberOverflow Status** This bit is set when the MSb of HcFmNumber (bit 15) changes value, from 0 to 1 or from 1 to 0, and after HccaFrameNumber has been updated.
4	RO	**UnrecoverableError Status** This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset. This event is not implemented and is hard-coded to '0'.
3	R/W	**ResumeDetected Status** This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the UsbResume state.
2	R/W	**StartofFrame Status** This bit is set by HC at each start of a frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
1	R/W	**WritebackDoneHead Status** This bit is set immediately after HC has written HcDoneHead to HccaDoneHead. Further updates of the HccaDoneHead will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of HccaDoneHead.
0	R/W	**SchedulingOverrun Status** This bit is set when the USB schedule for the current Frame overruns and after the update of HccaFrameNumber. A scheduling overrun will also cause the SchedulingOverrunCount of HcCommandStatus to be incremented.

Register 10h *HcInterruptEnable* Register

Default Value: 00000000h

Access: Read/Write

Each enable bit in the *HcInterruptEnable* register corresponds to an associated interrupt bit in the *HcInterruptStatus* register. The *HcInterruptEnable* register is used to control those events generate a hardware interrupt. When a bit is set in the *HcInterruptStatus* register AND the corresponding bit in the *HcInterruptEnable* register is set AND the **MasterInterruptEnable** bit is set, then a hardware interrupt is requested on the host bus.

Writing a '1' to a bit in this register sets the corresponding bit, whereas writing a '0' to a bit in this register leaves the corresponding bit unchanged. On read, the current value of this register is returned.

BIT	ACCESS	DESCRIPTION
31	R/W	**MasterInterrupt Enable** A '0' written to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as a Master Interrupt Enable.
30	R/W	**OwnershipChange Enable** 0 : Ignore 1 : Enable interrupt generation due to Ownership Change.
29:7		**Reserved**
6	R/W	**RootHubStatusChange Enable** 0 : Ignore 1: Enable interrupt generation due to Root Hub Status Change.
5	R/W	**FrameNumberOverflow Enable** 0 : Ignore 1 : Enable interrupt generation due to Frame Number Overflow.
4	R/W	**UnrecoverableError Enable** This event is not implemented. All writes to this bit will be ignored.
3	R/W	**ResumeDetected Enable** 0 : Ignore 1 : Enable interrupt generation due to Resume Detect.
2	R/W	**StartofFrame Enable** 0 : Ignore 1 : Enable interrupt generation due to Start of Frame.
1	R/W	**WritebackDoneHead Enable** 0 : Ignore 1 : Enable interrupt generation due to HcDoneHead Writeback
0	R/W	**SchedulingOverrun Enable** 0 : Ignore 1 : Enable interrupt generation due to Scheduling Overrun.

Register 14h *HcInterruptDisable* Register

Default Value: 00000000h

Access: Read/Write

Each disable bit in the *HcInterruptDisable* register corresponds to an associated interrupt bit in the *HcInterruptStatus* register. The *HcInterruptDisable* register is coupled with the *HcInterruptEnable* register. Thus, writing a '1' to a bit in this register clears the corresponding bit in the *HcInterruptEnable* register, whereas writing a '0' to a bit in this register leaves the corresponding bit in the *HcInterruptEnable* register unchanged. On read, the current value of the *HcInterruptEnable* register is returned.

BIT	ACCESS	DESCRIPTION
31	R/W	**MasterInterrupt Disable** A '0' written to this field is ignored by HC. A '1' written to this field disables interrupt generation due to events specified in the other bits of this register. This field is set after a hardware or software reset.
30	R/W	**OwnershipChange Disable** 0 : Ignore 1 : Disable interrupt generation due to Ownership Change.
29:7		**Reserved**
6	R/W	**RootHubStatusChange Disable** 0 : Ignore 1 : Disable interrupt generation due to Root Hub Status Change.
5	R/W	**FrameNumberOverflow Disable** 0 : Ignore 1: Disable interrupt generation due to Frame Number Overflow.
4	R/W	**UnrecoverableError Disable** This event is not implemented. All writes to this bit will be ignored.
3	R/W	**ResumeDetected Disable** 0 : Ignore 1 : Disable interrupt generation due to Resume Detect.
2	R/W	**StartofFrame Disable** 0 : Ignore 1 : Disable interrupt generation due to Start of Frame.
1	R/W	**WritebackDoneHead Disable** 0 : Ignore 1 : Disable interrupt generation due to HcDoneHead Writeback.

0	R/W	**Scheduling Overrun Disable** 0 : Ignore 1 : Disable interrupt generation due to Scheduling Overrun.

8.11 MEMORY POINTER PARTITION

Register 18h HcHCCA Register

Default Value: 00000000h

Access: Read/Write

The *HcHCCA* register contains the physical address of the Host Controller Communication Area. The Host Controller Driver determines the alignment restrictions by writing all 1s to *HcHCCA* and reading the content of *HcHCCA*. The alignment is evaluated by examining the number of zeroes in the lower order bits. The minimum alignment is 256 bytes; therefore, bits 0 through 7 must always return '0' when read. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.

BIT	ACCESS	DESCRIPTION
31:8	R/W	This is the base address of the Host Controller Communication Area.
7:0		**Reserved.**

Register 1Ch HcPeriodCurrentED Register

Default Value: 00000000h

Access: Read/Write

The HcPeriodCurrentED register contains the physical address of the current Isochronous or Interrupt Endpoint Descriptor.

BIT	ACCESS	DESCRIPTION
31:4	R/W	**PeriodCurrentED** This is used by HC to point to the head of one of the Periodic lists that will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.
3:0		**Reserved**

Register 20h *HcControlHeadED* Register

Default Value: 00000000h

Access: Read/Write

The *HcControlHeadED* register contains the physical address of the first Endpoint Descriptor of the Control list.

BIT	ACCESS	DESCRIPTION

31:4	R/W	**ControlHeadED** HC traverses the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0		**Reserved.**

Register 24h HcControlCurrentED Register

Default Value: 00000000h

Access: Read/Write

The HcControlCurrentED register contains the physical address of the current Endpoint Descriptor of the Control list.

BIT	ACCESS	DESCRIPTION
31:4	R/W	**ControlCurrentED** This pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled of in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.
3:0		**Reserved.**

Register 28h HcBulkHeadED Register

Default Value: 00000000h

Access: Read/Write

The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list.

BIT	ACCESS	DESCRIPTION
31:4	R/W	**BulkHeadED** HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0		**Reserved.**

Register 2Ch HcBulkCurrentED Register

Default Value: 00000000h

Access: Read/Write

The HcBulkCurrentED register contains the physical address of the current endpoint of the

Bulk list. As the Bulk list will be served in a round-robin fashion, the endpoints will be ordered according to their insertion to the list.

BIT	ACCESS	DESCRIPTION
31:4	R/W	**BulkCurrentED** This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the ControlListFilled of HcControl. If set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the BulkListEnable of HcControl is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
3:0		**Reserved.**

Register 30h HcDoneHead Register

Default Value: 00000000h

Access: Read/Write

The HcDoneHead register contains the physical address of the last completed Transfer Descriptor that was added to the Done queue. In normal operation, the Host Controller Driver should not need to read this register as its content is periodically written to the HCCA.

BIT	ACCESS	DESCRIPTION
31:4	R/W	**DoneHead** When a TD is completed, HC writes the content of HcDoneHead to the NextTD field of the TD. HC then overwrites the content of HcDoneHead with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the WritebackDoneHead of HcInterruptStatus.
3:0		**Reserved**

8.12 BITS FRAME COUNTER PARTITION

Register 34h HcFmInterval Register

Default Value: 00002EDFh

Access: Read/Write

The HcFmInterval register contains a 14-bit value which indicates the bit time interval in a Frame, (i.e., between two consecutive SOFs), and a 15-bit value indicating the Full Speed maximum packet size that the Host Controller may transmit or receive without causing scheduling overrun. The Host Controller Driver may carry out minor adjustment on the **FrameInterval** by writing a new value over the present one at each SOF. This provides the programmability necessary for the Host Controller to synchronize with an external clocking

resource and to adjust any unknown local clock offset.

BIT	ACCESS	DESCRIPTION
31	R/W	**FrameIntervalToggle** HCD toggles this bit whenever it loads a new value to FrameInterval.
30:16	R/W	**FSLargestDataPacket** This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
15:14		**Reserved**
13:0	R/W	**FrameInterval** This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of HcCommandStatus as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.

Register 38h HcFmRemaining Register

Default Value: 00000000h

Access: Read Only

The HcFmRemaining register is a 14-bit down counter showing the bit time remaining in the current Frame.

BIT	ACCESS	DESCRIPTION
31	RO	**FrameRemainingToggle** This bit is loaded from the FrameIntervalToggle field of HcFmInterval whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.
30:14		**Reserved**
13:0	RO	**FrameRemaining** This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in HcFmInterval at the next bit time boundary. When entering the UsbOperational state, HC re-loads the content with the FrameInterval of HcFmInterval and uses the updated value from the next SOF.

Register 3Ch HcFmNumber Register

Default Value: 00000000h

Access: Read

The HcFmNumber register is a 16-bit counter. It provides a timing reference among events occurring in the Host Controller and the Host Controller Driver. The Host Controller Driver may use the 16-bit value specified in this register and generate a 32-bit frame number without requiring frequent access to the register.

BIT	ACCESS	DESCRIPTION
31:16		**Reserved**
15:0	RO	**FrameNumber** This is incremented when HcFmRemaining is re-loaded. It will be rolled over to 0h after ffffh. When entering the UsbOperational state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the FrameNumber at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the StartofFrame in HcInterruptStatus.

Register 40h HcPeriodicStart Register

Default Value: 00000000h

Access: Read/Write

The HcPeriodicStart register has a 14-bit programmable value which determines when is the earliest time HC should start processing the periodic list.

BIT	ACCESS	DESCRIPTION
31:14		**Reserved**
13:0	R/W	**PeriodicStart** After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from HcFmInterval. A typical value will be 3E67h. When HcFmRemaining reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

Register 44h HcLSThreshold Register

Default Value: 00000000h

Access: Read/Write

The HcLSThreshold register contains an 11-bit value used by the Host Controller to determine whether to commit to the transfer of a maximum of 8-byte LS packet before EOF. Neither the Host Controller nor the Host Controller Driver are allowed to change this value.

BIT	ACCESS	DESCRIPTION
31:12		**Reserved**
11:0	R/W	**LSThreshold** This field contains a value which is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining ≥ this field. The value is calculated by HCD with the consideration of transmission and setup overhead.

8.13 ROOT HUB PARTITION

All registers included in this partition are dedicated to the USB Root Hub which is an integral part of the Host Controller though still a functionally separate entity. The HCD emulates USBD accesses to the Root Hub via a register interface. The HCD maintains many USB-defined hub features which are not required to be supported in hardware. For example, the Hub's Device, Configuration, Interface, and Endpoint Descriptors are maintained only in the HCD as well as some static fields of the Class Descriptor. The HCD also maintains and decodes the Root Hub's device address as well as other trivial operations which are better suited to software than hardware.

The Root Hub register interface is otherwise developed to maintain similarity of bit organization and operation to typical hubs which are found in the system. Below are four register definitions: HcRhDescriptorA, HcRhDescriptorB, HcRhStatus, and HcRhPortStatus[5:1]. Each register is read and written as a Dword. These registers are only written during initialization to correspond with the system implementation. The HcRhDescriptorA and HcRhDescriptorB registers should be implemented such that they are writable regardless of the HC USB state. HcRhStatus and HcRhPortStatus must be writable during the USBOPERATIONAL state.

Register 48h HcRhDescriptorA Register

Default Value: 01000005h

Access: Read/Write

The HcRhDescriptorA register is the first register of two describing the characteristics of the Root Hub. Reset values are implementation-specific. The descriptor length (11), descriptor type (TBD), and hub controller current (0) fields of the hub Class Descriptor are emulated by the HCD. All other fields are located in the HcRhDescriptorA and HcRhDescriptorB registers.

BIT	ACCESS	DESCRIPTION
31:24	R/W	**PowerOnToPowerGoodTime** This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2 ms.
23: 13		**Reserved**

12	R/W	**NoOverCurrentProtection** This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting. 0 : Over-current status is reported collectively for all downstream ports 1 : No overcurrent protection supported
11	R/W	**OverCurrentProtectionMode** This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, this fields should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared. 0 : over-current status is reported collectively for all downstream ports 1 : over-current status is reported on a per-port basis
10	RO	**DeviceType** This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.
9	R/W	**NoPowerSwitching** These bits are used to specify whether power switching is supported or port are always powered. SiS5595 USB HC supports global power switching mode. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching. 0 : Ports are power switched 1 : Ports are always powered on when the HC is powered on
8	R/W	**PowerSwitchingMode** This bit is used to specify how the power switching of the Root Hub ports is controlled. SiS5595 USB HC supports global power switching mode. This field is only valid if the NoPowerSwitching field is cleared. 0 : all ports are powered at the same time. 1 : Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ Clear Global Power).

7:0	RO	**NumberDownstreamPorts** These bits specify the number of downstream ports supported by the Root Hub. SiS960 USB HC supports five downstream ports.

Register 4Ch HcRhDescriptorB Register

Default Value: 00000000h

Access: Read/Write

The HcRhDescriptorB register is the second register of two describing the characteristics of the Root Hub. These fields are written during initialization to configure the Root Hub.

BIT	ACCESS	DESCRIPTION
31:16	R/W	**PortPowerControlMask** Each bit indicates if a port is affected by a global power control command when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode=0), this field is not valid. SiS5595 USB HC implements global power switching. bit 0: Reserved bit 1: Ganged-power mask on Port #1 bit 2: Ganged-power mask on Port #2 ... bit15: Ganged-power mask on Port #15
15:0	R/W	**DeviceRemovable** Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. bit 0: Reserved bit 1: Device attached to Port #1 bit 2: Device attached to Port #2 ... bit15: Device attached to Port #15

Register 50h HcRhStatus Register

Default Value: 00000000h

Access: Read/Write

The HcRhStatus register is divided into two parts. The lower word of a Dword represents the Hub Status field and the upper word represents the Hub Status Change field. Reserved bits should always be written '0'.

BIT	ACCESS	DESCRIPTION
31	WO	**ClearRemoteWakeupEnable(Write)** Writing a '1' clears DeviceRemoveWakeupEnable. Writing a '0' has no effect.
30:18		**Reserved**
17	R/W	**OverCurrentIndicatorChange** This bit is set by hardware when a change has occurred to the OCI field of this register. The HCD clears this bit by writing a '1'.Writing a '0' has no effect.
16	R/W	**LocalPowerStatusChange(Read)** The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. **SetGlobalPower(Write)** In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.
15	R/W	**DeviceRemoteWakeupEnable(Read)** This bit enables a ConnectStatusChange bit as a resume event, causing a UsbSuspend to UsbResume state transition and setting the ResumeDetected interrupt. 0 : **ConnectStatusChange** is not a remote wakeup event. 1 : **ConnectStatusChange** is a remote wakeup event. **SetRemoteWakeupEnable(Write)** Writing a '1' sets DeviceRemoveWakeupEnable. Writing a '0' has no effect.
14:2		**Reserved**
1	RO	**OverCurrentIndicator** This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always '0'

0	R/W	**LocalPowerStatus((Read))** The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. **ClearGlobalPower(Write)** In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.

Register 54h/58h/5Ch/60h/64h HcRhPortStatus[5:1] Register

Default Value: 00000000h

Access: Read/Write

The HcRhPortStatus[5:1] register is used to control and report port events on a per-port basis. Five HcRhPortStatus registers that are implemented in hardware. The lower word is used to reflect the port status, whereas the upper word reflects the status change bits. Some status bits are implemented with special write behavior (see below). If a transaction (token through handshake) is in progress when a write to change port status occurs, the resulting port status change must be postponed until the transaction completes. Reserved bits should always be written '0'.

BIT	ACCESS	DESCRIPTION
31:21		**Reserved**
20	R/W	**PortResetStatusChange** This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 : port reset is not complete 1 : port reset is complete
19	R/W	**PortOverCurrentIndicatorChange** This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 : no change in PortOverCurrentIndicator 1 : PortOverCurrentIndicator has changed

18	R/W	**PortSuspendStatusChange** This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when ResetStatusChange is set. 0 : resume is not completed 1 : resume completed
17	R/W	**PortEnableStatusChange** This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 : no change in **PortEnableStatus** 1 : change in PortEnableStatus
16	R/W	**ConnectStatusChange** This bit is set whenever a connect or disconnect event occurs. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared when a SetPortReset, SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected. 0 : no change in CurrentConnectStatus 1 : change in CurrentConnectStatus Note: If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.
15:10		**Reserved**
9	R/W	**LowSpeedDeviceAttached((Read))** This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set. 0 : full speed device attached 1 : low speed device attached

8	R/W	**Port Power Status((Read))** This bit reflects the port's power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing Set Port Power or Set Global Power. HCD clears this bit by writing Clear Port Power or Clear Global Power. Which power control switches are enabled is determined by Power Switching Mode and Port Port Control Mask[NDP]. In global switching mode (Power Switching Mode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (Power Switching Mode=1), if the Port Power Control Mask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ Clear Global Power commands are enabled. When port power is disabled, Current Connect Status, Port Enable Status, Port Suspend Status, and Port Reset Status should be reset. 0 : port power is off 1 : port power is on **SetPortPower(Write)** The HCD writes a '1' to set the PortPowerStatus bit. Writing a '0' has no effect. Note: This bit is always reads '1b' if power switching is not supported.
7:5		**Reserved**
4	R/W	**PortResetStatus(Read)** When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared. 0 : port reset signal is not active 1 : port reset signal is active **SetPortReset(Write)** The HCD sets the port reset signaling by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.

3	R/W	**PortOverCurrentIndicator(Read)** This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal 0 : no overcurrent condition. 1 : overcurrent condition detected. **ClearSuspendStatus(Write)** The HCD writes a '1' to initiate a resume. Writing a '0' has no effect. A resume is initiated only if PortSuspendStatus is set.
2	R/W	**PortSuspendStatus(Read)** This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the UsbResume state. If an upstream resume is in progress, it should propagate to the HC. 0 : port is not suspended 1 : port is suspended **SetPortSuspend(Write)** The HCD sets the PortSuspendStatus bit by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.

1	R/W	**PortEnableStatus(Read)** This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set. 0 : port is disabled 1 : port is enabled **SetPortEnable(Write)** The HCD sets PortEnableStatus by writing a '1'.Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected port.
0	R/W	**CurrentConnectStatus(Read)** This bit reflects the current state of the downstream port. 0 : no device connected 1 : device connected **ClearPortEnable(Write)** The HCD writes a '1' to this bit to clear the PortEnableStatus bit. Writing a '0' has no effect. The CurrentConnectStatus is not affected by any write. Note: This bit is always read ‘1b’ when the attached device is nonremovable (DeviceRemoveable[NDP]).

8.14 LEGACY SUPPORT REGISTERS

Four operational registers are used to provide the legacy support . Each of these registers is located on a 32-bit boundary. The offset of these registers is relative to the base address of the Host Controller operational registers with HceControl located at offset 100h.

Table 8.14-1 Legacy Support Registers

OFFSET	REGISTER	DESCRIPTION
100h	HceControl	Used to enable and control the emulation hardware and report various status informations.

104h	HceInput	Emulation side of the legacy Input Buffer register.
108h	HceOutput	Emulation side of the legacy Output Buffer register where keyboard and mouse data is to be written by software.
10Ch	HceStatus	Emulation side of the legacy Status register.

Three of the operational registers (HceStatus, HceInput, HceOutput) are accessible at I/O address 60h and 64h when emulation is enabled. Reads and writes to the registers using I/O addresses have side effects as outlined in the Table 8.14-2 Emulated Registers

Table 8.14-2 Emulated Registers

I/O ADDRESS	CYCLE TYPE	REGISTER CONTENTS ACCESSED /MODIFIED	SIDE EFFECTS
60h	IN	HceOutput	IN from port 60h will set OutputFull in HceStatus to 0
60h	OUT	HceInput	OUT to port 60h will set InputFull to 1 and CmdData to 0 in HceStatus.
64h	IN	HceStatus	IN from port 64h returns current value of HceStatus with no other side effect.
64h	OUT	HceInput	OUT to port 64h will set InputFull to 0 and CmdData in HceStatus to 1.

Register 100h HceControl Register

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:9		**Reserved**
8	R/W	**A20State** Indicates current state of Gate A20 on keyboard controller. Used to compare against value to 60h when GateA20Sequence is active.
7	R/W	**IRQ12Active** Indicates that a positive transition on IRQ12 from keyboard controller has occurred. SW may write a 1 to this bit to clear it (set it to 0). SW write of a 0 to this bit has no effect.
6	R/W	**IRQ1Active** Indicates that a positive transition on IRQ1 from keyboard controller has occurred. SW may write a 1 to this bit to clear it (set it to 0). SW write of a 0 to this bit has no effect.

5	R/W	**GateA20Sequence** Set by HC when a data value of D1h is written to I/O port 64h. Cleared by HC on write to I/O port 64h of any value other than D1h.
4	R/W	**ExternalIRQEn** When set to 1, IRQ1 and IRQ12 from the keyboard controller causes an emulation interrupt. The function controlled by this bit is independent of the setting of the **EmulationEnable** bit in this register.
3	R/W	**IRQEn** When set, the HC generates IRQ1 or IRQ12 as long as the **OutputFull** bit in *HceStatus* is set to 1. If the **AuxOutputFull** bit of *HceStatus* is 0, then IRQ1 is generated; if it is 1, then an IRQ12 is generated.
2	R/W	**CharacterPending** When set, an emulation interrupt is generated when the **OutputFull** bit of the *HceStatus* register is set to 0.
1	RO	**EmulationInterrupt** This bit is a static decode of the emulation interrupt condition
0	R/W	**EmulationEnable** When set to 1, the HC is enabled for legacy emulation. The HC decodes accesses to I/O registers 60h and 64h and generates IRQ1 and/or IRQ12 when appropriate. Additionally, the HC generate s an emulation interrupt at appropriate times to invoke the emulation software.

Register 104h HceInput Register

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:8		**Reserved**
7:0	R/W	**InputData** This register holds data that is written to I/O ports 60h and 64h. I/O data that is written to ports 60h and 64h is captured in this register when emulation is enabled. This register may be read or written directly by accessing it with its memory address in the Host Controller's operational register space. When accessed directly with a memory cycle, reads and writes of this register have no side effects.

Register 108h HceOutput Register

Default Value: 00000000h

Access: Read/write

BIT	ACCESS	DESCRIPTION
31:8		**Reserved**
7:0	R/W	**OutputData** This register hosts data that is returned when an I/O read of port 60h is performed by application software. The data placed in this register by the emulation software is returned when I/O port 60h is read and emulation is enabled. On a read of this location, the OutputFull bit in HceStatus is set to 0.

Register 10Ch HceStatus Register

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:8		**Reserved**
7	R/W	**Parity** Indicates parity error on keyboard/mouse data.
6	R/W	**Time-out** Used to indicate a time-out
5	R/W	**AuxOutputFull** IRQ12 is asserted whenever this bit is set to 1 and **OutputFull** is set to 1 and the **IRQEn** bit is set.
4	R/W	**Inhibit Switch** This bit reflects the state of the keyboard inhibit switch and is set if the keyboard is NOT inhibited.
3	R/W	**CmdData** The HC sets this bit to 0 on an I/O write to port 60h and to 1 on an I/O write to port 64h
2	R/W	**Flag** Nominally used as a system flag by software to indicate a warm or cold boot.
1	R/W	**InputFull** Except for the case of a Gate A20 sequence, this bit is set to 1 on an I/O write to address 60h or 64h. While this bit is set to 1 and emulation is enabled, an emulation interrupt condition exists.

0	R/W	**OutputFull** The HC sets this bit to 0 on a read of I/O port 60h. If **IRQEn** is set and **AuxOutputFull** is set to 0, then an IRQ1 is generated as long as this bit is set to 1. If **IRQEn** is set and **AuxOutputFull** is set to 1, then an IRQ12 is generated as long as this bit is set to 1. While this bit is 0 and **CharacterPending** in *HceControl* is set to 1, an emulation interrupt condition exists. The contents of the *HceStatus* Register are returned on an I/O Read of port 64h when emulation is enabled. Reads and writes of port 60h and writes to port 64h can cause changes in this register. Emulation software can directly access this register through its memory address in the Host Controller's operational register space. Accessing this register through its memory address produces no side effects.

8.15 PCI CONFIGURATION REGISTER MAP:

Table 8.15-1 PCI Configuration Register Map

Offset	+3h	+2h	+1h	+0h
00h	Device ID		Vendor ID	
04h	Status		Command	
08h	Class Code			Revision ID
0Ch	BIST	Header Type	Latency Timer	Cache Line Size
10h	Audio IO Base Address			
14h	Audio Memory Base Address			
18-28h	RSVD			
2Ch	Subsystem ID		Subsystem Vendor ID	
30h	RSVD			
34h	RSVD			Cap_Ptr
38h	RSVD			
3Ch	MAX_LAT	MIN_GNT	Interrupt Pin	Interrupt Line
40h	DDMA Slave CFG			
44h	PM_Timer	PM_CFG	LEGACY_DMA	LEGACY_IOBASE
48h	RSVD		INT_VEC	INTA_SNOOP_ENA
DCh	PMC		PM_Next_Ptr	PM_Cap_ID
E0h	Power Value Data	PMCSR_BSE	PMCSR	

Register 00h Device ID & Vendor ID

Default Value: ????????h

Access: read/write, can be written only when CFG46h[6]=1

BIT	ACCESS	DESCRIPTION
31:16	R/W	device ID: default ????h
15:0	R/W	vendor ID: default 1039h

Register 04h Status & Command

Default: 02900000h

Description: Read/Write

BIT	ACCESS	DESCRIPTION
2:0	R/W	

28	R/W	TA	Received target abort. Write 1 to clear.
29	R/W	MA	Received master abort. Write 1 to clear.
20	R/W	PM	PCI Power Management support, hardwired to 1
23:25	R/W	hardwired to 1 The rest bits : hardwired to 0	

Register 08h-0Bh Status & Command

Default Value: 04010001h

Access: read only

BIT	ACCESS	DESCRIPTION	
7:0	RO	01	revision ID
31:24	RO	04	Base class: Multimedia
23:16	RO	01	Sub-class: Audio device
15:8	RO	00	Interface:

Register 0Ch BIST, Header Type, Latency Timer & Cache Line Size Legacy Address:

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
15:12	R/W	The rest bits : hardwired to 0

Register 10h Audio IO Base Register:

Default Value: 00000001h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:8	R/W	Audio IO base
7:1	R/W	Hardwire to 0
0	R/W	Hardwire to 1

Register 14h Audio MEM Base Register:

Default Value: **00000000h**

Access: **Read/Write**

BIT	ACCESS	DESCRIPTION
31:12	R/W	Audio MEM base

11:0	R/W	Hardwire to 0

Register 2Ch Subsystem ID & Subsystem vendor ID:

Legacy Address:

Default Value: 001B100Bh

Access: read/write, can be written only when CFG46h[6]=1

BIT	ACCESS	DESCRIPTION
31:16	R/W	subsystem ID: default ????h
15:0	R/W	subsystem vendor ID: default ????h

Register 34h PCIPM Capability List Pointer Register:

Default Value: 000000DCh

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	PCIPM Capability List Pointer Register

Register 3Ch Max_Lat, Min_Gnt, Interrupt Pin & Interrupt Line:

Default Value: 18020100h

Access: Read /Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	INT line
15:8	R/W	INT pin hardwired to 01
23:16	R/W	Min_Gnt hardwired to 02
31:24	R/W	Max_Gnt hardwired to 18

Register 40h DDMA Slave Configuration Register:

Default Value: 00000000h

Access: Read /Write

BIT	ACCESS	DESCRIPTION
31:4	R/W	DDMABase
3	R/W	Non Legacy Extended Addressing Control (Fully 32 bit Addressing) 0: disabled 1: enabled

2:1	R/W	Legacy DMA Transfer Size Control, Read Only as 00 00:8 bit transfer, legacy
0	R/W	DDMA Slave Channel Access Enable Control 0: disabled 1: enabled When disabled, the DDMABase is not usefull and the PCM sample playback control registers can not be accessed through DDMA Slave channel method. When enabled, TSAudio can behave like a DDMA Slave channel device. DDMA Master will transfer the legacy DMA controller channel specific information to the related DDMA Slave channel control register when software trying to program the legacy DMA controller register.

Register 44h legacy I/O decoding

Default Value: E2000000h

Access: Read /Write

BIT	ACCESS	DESCRIPTION
7	R/W	0: MPU401Base disable 1: MPU401Base enable
6	R/W	0: MPU401Base = 0330h-0333h 1: MPU401Base = 0300h-0303h
5	R/W	0: GAMEBase disable 1: GAMEBase enable
4	R/W	0: GAMEBase = 0200h-0207h 1: GAMEBase = 0208h-020Fh
3	R/W	0: ADLIBBase disable 1: ADLIBBase enable
2	R/W	0: ADLIBBase = 0388h-038Bh 1: ADLIBBase = 038Ch-038Fh
1	R/W	0: SBBase disable 1: SBBase enable
0	R/W	0: SBBase = 0220h-022Fh 1: SBBase = 0240h-024Fh

Register 45h legacy DMA decoding

Default Value: E2000000h

Access: Read /Write

BIT	ACCESS	DESCRIPTION
5:7	R/W	reserved
4	R/W	DMAREG_RD_EN_ 0: Response to DMAREG(00h-03h, 83h/87h) Read when CFG45[1] is 1; 1: Never response to DMAREG(00h-03h, 83h/87h) Read.
3	R/W	0: DMA status retry OK 1: DMA status retry error If bit3 is set, bus interface will not respond to IO8 operation any more unless the status retry error bit is cleared by writing 1 to this bit.
2	R/W	0: DMA status handle mode A (slave only) 1: DMA status handle mode B (bus master)
1	R/W	0: DMA trapping disable 1: DMA trapping enable
0	R/W	0: DMA channel 1 trapping 1: DMA channel 0 trapping

when DMA trapping is enable, chip will decode the following I/O port

DMA channel 1 trapping

read	2,3
write snoop	2,3
write snoop	8-Fh
write snoop	83h

DMA channel 0 trapping

read	0,1
write snoop	0,1
write snoop	8-Fh

write snoop 87h

when DMA trapping is enable, chip will handle DMA status read (I/O read port 8) depend on the DMA status mode bit.

- DMA status handle mode A:

9783 will decode I/O read port 8 if StatusRDY is active, otherwise, it will ignore the cycle.

- DMA status handle mode B:

When StatusRDY is not active, chip will retry DMA status read if it is not the current active bus master. Whenever chip retry the DMA status read from other bus master, it will also generate an bus request for the DMA status read. When the DMA status read cycle generated by chip is terminated normally, chip will write the status data by assert the StatusWR signal.

If chip retry DMA status read from other bus master 3 times without getting the bus ownership or proper data, it will set the status error bit high which will terminate the pending DMA status read request internally and ignore the all DMA status read cycle by the other bus master.

When audio engine receive the StatusWR signal, it will assert the StatusRDY signal to chip and allow chip to decode I/O read port 8 normally. The audio engine will de-assert the StatusRDY after each DMA status read.

NOTE:

All I/O decoding is 16 bit, write snooping happen only once even with multiple write retry cycle. Write snooping means chip will decode the cycle to audio engine without generate the DEVSEL# signal or TRDY# to PCI bus.

Register 46h Power Management Configuration (PM_CFG)

Default Value: 00h

Access: Read /Write

BIT	ACCESS	DESCRIPTION
7	R/W	(TIMER_PME_EN) Inactivity Timer assert PME# enable

		0: Disable 1: Enable If enabled, when Inactivity Timer expired, PME# will be asserted.
6	R/W	(ID_WR_EN) Chip IDs write enable 0:Vendor ID, Device ID, Subsystem vendor ID & Subsystem ID are read only 1:Vendor ID, Device ID, Subsystem vendor ID & Subsystem ID are writable. Bit 7 (TIMER_PME_EN) Inactivity Timer assert PME# enable
5	R/W	(WAKE_EN2) Secondary CODEC Wake-up Enable Read/Write. Powered with Vaux. Cleared when H/W reset or S/W reset. 0: disable 1: enable When CODEC_PD = 1, BCLK keeps low, a rising edge of ACDI2 will set WAVE_EV to high
4	R/W	(WAKE_EN1) Primary CODEC Wake-up Enable Read/Write. Powered with Vaux. Cleared when H/W reset or S/W reset. 0: Disable 1: Enable When CODEC_PD = 1, BCLK keeps low, a rising edge of ACDI1 will set WAVE_EV to high
3	R/W	(AC_PM_EN_) Analog CODEC Power Management Enable 0: Enable If enabled, AC97 bit clock can be shut off according to PM_ST 1: Disable
2	R/W	(DC_RST) Digital Controller Software Reset 0:normal 1:Reset Digital Controller
1	R/W	(DC_PM_EN_) Digital Controller Power Management Enable 0:Enable When enabled, Audio_clk can be shut off or turn on according to PM_ST.

		1:Disable
0	R/W	(DCC_EN) Dynamic Clock Control Enable 0:Disable 1:Enable. CLKRUN# scheme will be enabled.

Register 47h Inactivity Timer Expiration Control

Default Value: 00h

Access: Read /Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	Inactivity timer expiration base (in second) Each time when audio engine enters into D2 state, the Inactivity timer will load the base count from this register and start counting at 1s clock rate. When the MSB of the counter goes from high to low, The timer expired. When not at D2 state, the timer is reset.

Register 48h INT Acknowledge Snoop Register:

Default Value: 00h

Access: Read /Write

BIT	ACCESS	DESCRIPTION
15:7	R/W	(INT_VEC) Interrupt Vector to be matched
0	R/W	(INTA_SNOOP_ENA) Interrupt Acknowledge Snooping Enable bit. 0:Disable 1:Enable

Register DCh Power management capability register (PMC)

Default Value: 66010001h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	(PM_Cap_ID) Power management capability identifier , read only as 01h
15:8	RO	(PM_Next_Ptr) Next data structure item list pointer in the PCI header, read only as 00h
31:16	RO	(PM_CAP) Power management capability register, read only as E611h.

31:27	RO	(PME_Support) PME# supported PM_ST, read only as 01100b, indicates that PME# can be asserted in D2, D3hot.
26	RO	(D2_Support) Read only as 1, indicates D2 supported.
25	RO	(D1_Support) Read only as 1, indicates D1 supported.
24:22	RO	Reserved. Read only as 000b
21	RO	(DSI) Device Specific Initialization. Read only as 0.
20	RO	(Vaux) Auxiliary Power Source. Read only as 0.
19	RO	(PME_clk) PME clock. Read only as 0, indicates that no PCI clock is required to generate PME#.
18:16	RO	(Version)Read only as 001b, indicates PPMI v1.0 compliance

Register E0h Power management control/status register (PMCSR) & PMCSR_BSE & Data:

Default Value: 00000000h

Access: Read /Write

BIT	ACCESS	DESCRIPTION
31:24	R/W	(Data) Read only as 00h.
23:16	R/W	(PMCSR_BSE) Read only as 00h.
15:0	R/W	(PMCSR) Power Management Control/Status Register
15	R/W	(PME_Status) Read/Write-Clear. 0:(Default) Normal (PME# is controlled by bit[8] PME_En) 1:PME# can be asserted independent of bit[8] (PME_En). Writing 0 to this bit has no effectt. Writing 1 to this bit will clear this bit, and also cause chip to stop asserting PME#.
14:13	R/W	(Data_Scale) Read only as 00b.
12:9	R/W	(Data_Select) Read only as 0000b
8	R/W	(PME_En) Read/Write. 0:(Default) PME# is disabled to be asserted. 1:PME# is enabled to be asserted.
7:2	R/W	Reserved. Read only as 000000b
1:0	R/W	(PM_ST) Power State. Read/Write. Read will return current Power State, write will set to new state.

		00 D0 01 D1 10 D2 11 D3hot

8.16 AUDIO PROCESSOR REGISTER MAP:

Table 8.16-1 Audio Processor Register Map

IO Offset	+3h	+2h	+1h	+0h
00h	DMAR3	DMAR2	DMAR1	DMAR0
04h	DMAR7	DMAR6	DMAR5	DMAR4
08h	DMAR11	DMAR10	DMAR9	DMAR8
0Ch	DMAR15	DMAR14	DMAR13	DMAR12
10h	SBR3/SBR1	SBR2	SBR1/SBR3	SBR0
14h	RSVD	SBR6	SBR5	SBR4
18h	RSVD	SBR7	RSVD	RSVD
1Ch	SBR10	SBR9	RSVD	SBR8
20h	MPUR3	MPUR2	MPUR1	MPUR0
24h-2Ch	RSVD			
30h	RSVD	RSVD	GAMER1	GAMER0
34h	GAMER2			
38h	GAMER3			
3Ch	RSVD			
40h	ACWR			
44h	ACRD			
48h	SCTRL			
4Ch	ACGPIO			
50h	ASR0			
54h	RSVD	ASR2	RSVD	ASR1
58h	ASR3			
5Ch	ASR6	ASR5	RSVD	ASR4
60h	AOPLSR0			
70h	SPDIF_CS			
74h	RSVD			
78h	RSVD			

7Ch	RSVD	GPcontrol	GPO	GPI
80h	START_A			
84h	STOP_A			
88h	DLY			
8Ch	SIGN_CSO			
90h	CSPF_A			
94h	CEBC			
98h	AIN_A			
9Ch	EINT			
A0h	GC			CIR
A4h	AINTEN_A			
A8h	MUSICVOL		WAVEVOL	
ACh	SBDELTA/SBDELTA_R		RSVD	
B0h	MISCINT			
B4h	START_B			
B8h	STOP_B			
BCh	CSPF_B			
C0h	SBDMAL		SBDMAC	
C4h	SBE2R	RSVD	SBDD	SBCTRL
C8h	STIMER			
CCh	LFO_CTRL_B	LFO_CT_B	RSVD + I^2S_DELTA	
D0h	ST_TARGET			
D4h	RSVD			
D8h	AINT_B			
DCh	AINTEN_B			
Bank A: Channel Register				
ARAM_A (CIR<32)				
E0h	CSO		FMS+ALPHA(11:8)	ALPHA(7:0)
E4h	CPTR + LBA			
E8h	ESO		DELTA	
ECh	LFO_CTRL	LFO_CT	FMC+RVOL[6:1]	RVOL[0]+CVOL
ERAM_A (CIR<32)				
F0h	GVSEL + PAN	VOL	CTRL + Ec(11:8)	Ec(7:0)
F4h	EBUF1			

F8h	EBUF2			
FCh	RSVD			
Bank B: Channel Register				
ARAM_B (CIR>=32)				
E0h	CSO		FMS+ALPHA(11:8)	ALPHA(7:0)
E4h	CPTR + LBA			
E8h	ESO		DELTA	
ECh	ATTRIBUTE		FMC+RVOL[6:1]	RVOL[0]+CVOL
ERAM_B (CIR>=32)				
F0h	GVSEL + PAN	LFO_INIT(Bank A)	CTRL + VOL(11:8)	VOL(7:0)
F4h	RSVD			
F8h	RSVD			
FCh	RSVD			

Register 0h DMAR0 (Legacy DMA Playback Buffer Base Register Port 1)

Legacy Address: DDMASlaveBase + 0h || 0000h / 0002h

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	Legacy DMA Playback Buffer Current Transfer Address 7-0 The PCI bus interface circuit should response to I/O read to 0000h or 0002h on the PCI bus only when DMASnoopEn is active Legacy DMA Playback Buffer Base Address 7-0 Legacy DMA Playback Buffer Current Transfer Address 7-0

Register: 1h DMAR1 (Legacy DMA Playback Buffer Base Register Port 2)

Legacy Address: DDMASlaveBase + 1h || 0000h / 0002h

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	Legacy DMA Playback Buffer Current Transfer Address 15-8 The PCI bus interface circuit should response to I/O read to 0000h or 0002h on the PCI bus only when DMASnoopEn is active Legacy DMA Playback Buffer Base Address 15-8 Legacy DMA Playback Buffer Current Transfer Address 15-8

Register: 2h DMAR2 (Legacy DMA Playback Buffer Base Register Port 3)

Legacy Address: DDMASlaveBase + 2h || 0087h / 0083h

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	Legacy DMA Playback Buffer Current Transfer Address 23-16 The PCI bus interface circuit should response to I/O read to 0087h or 0083h on the PCI bus only when DMASnoopEn is active Legacy DMA Playback Buffer Base Address 23-16 Legacy DMA Playback Buffer Current Transfer Address 23-16

Register: 3h DMAR3 (Legacy DMA Playback Buffer Base Register Port4)

Legacy Address: DDMASlaveBase + 3h

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	Legacy DMA Playback Buffer Current Transfer Address 31-24 Legacy DMA Playback Buffer Base Address 31-24 Legacy DMA Playback Buffer Current Transfer Address 31-24

This register is intended for system which has DDMA Master.

Any time when legacy DMA playback is not running, this register must be reset to 0 by software driver.

Register: 4h DMAR4 (Legacy DMA Playback Byte Count Register 1)

Legacy Address: DDMASlaveBase + 4h || 0001h / 0003h

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	Legacy DMA Playback Current Byte Count 7-0 The PCI bus interface circuit should response to I/O read to 0003h or 0001h on the PCI bus only when DMASnoopEn is active Legacy DMA Playback Byte Base Count 7-0 Legacy DMA Playback Current Byte Count 7-0

Register: 5h DMAR5 (Legacy DMA Playback Byte Count Register 2)

Legacy Address: DDMASlaveBase + 5h || 0001h / 0003h

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	Legacy DMA Playback Current Byte Count 15-8 The PCI bus interface circuit should response to I/O read to 0003h or 0001h on the PCI bus only when DMASnoopEn is active. Legacy DMA Playback Byte Base Count 15-8 Legacy DMA Playback Current Byte Count 15-8

Register: 6h DMAR6 (Legacy DMA Playback Byte Count Register 3)

Legacy Address: DDMASlaveBase + 6h

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	Legacy DMA Playback Current Byte Count 23-16 Legacy DMA Playback Byte Base Count 23-16 Legacy DMA Playback Current Byte Count 23-16

This register is intended for system which has DDMA Master.

Any time when legacy DMA playback is not running, this register must be reset to 0 by software driver.

Register: 7h DMAR7(Legacy DMA Playback Misc. Register)

Legacy Address: DDMASlaveBase + 7h

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	

Register: 8h DMAR8(Legacy DMA Controller Command / Status Register)

Legacy Address: DDMASlaveBase + 8h || 0008h

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION

7:0	RO	status register for implemented legacy 8237-A DMA channel. Implementation of this register maintains the compatibility with legacy 8237-A status register. However, when reading this register, the return value should bedifferent for I/O read to (DDMASlaveBase + 8h) , I/O read to (AudioBase +8h)and I/O read to (0008h). I/O read to (DDMASlaveBase + 08h) is normallyinitiated by DDMA Master. I/O read to (AudioBase + 08h) is normally initiatedby our debug program. The DDMA Master will take the responsibility to combine the return value of each DMA Slave Channel in the system and return the finalresultant byte to response to the PCI I/O read to 0008h initiated by Host/PCIBridge. The PCI bus interface circuit should response to I/O read to 0008h on thePCI bus only when DMASnoopEn is active.

Register: Ah DMAR10(Legacy DMA Single Channel Mask Port)

Legacy Address: 000Ah

Default Value: 00h

Access: Write Only

BIT	ACCESS	DESCRIPTION
0	WO	channel mask register for implemented legacy 8237-A DMA channel . Writing to this register will affect the legacy DMA operation of TSAudio , implementation of this register maintains the register compatibility with legacy 8237-A DMA signal channel mask register . For system which has DDMA Master, it is the DMA Master's responsibility to update the legacy channel mask bit DMAR15.0 with address (DMASlaveBase + Fh) when a I/O write to 000Ah occurred on PCI Bus. When snooping legacy 8237-A register operation is enabled, any I/O write to 000Ah should be snooped to DMAR15.0 if the channel number matches the snooping legacy DMA channel number..

Register: 0Bh DMAR11(Legacy DMA Channel Operation Mode Register)

Legacy Address: DDMASlaveBase + 0Bh || 000Bh

Default Value: 00h

Access: Read / Write

BIT	ACCESS	DESCRIPTION
7:0	RW	This register can only be read out through AudioBase + 0Bh port

		channel mode register for implemented legacy 8237-A DMA channel . Writing to this register will affect the legacy DMA operation of TSAudio , implementation of this register maintains the register compatibility with legacy 8237-A DMA channel mode register for system with or without DDMA Master . For system which has DDMA Master, it is the DMA Master's responsibility to update this register when a I/O write to 000Bh occurred on PCI Bus. When snooping legacy 8237-A register operation is enabled, any I/O write to 000Bh should be snooped to this register if the channel number matches the snooping legacy DMA channel number.

Register: Ch DMAR12(Legacy DMA Controller First_Last Flag Clear Port)

Legacy Address: 000Ch

Default Value:

Access: Write Only

BIT	ACCESS	DESCRIPTION
0	WO	first_last flag clear register for implemented legacy 8237-A DMA channel . Writing to this register will clear the flag signal First_Last. Implementation of this register maintains the register compatibility with legacy 8237-A DMA controller for system without DDMA Master. For system which has DDMA Master, it is the DMA Master's responsibility to implement this flag. When snooping legacy 8237-A register operation is enabled, any I/O write to 000Ch should clear First_Last flag

Register: Dh DMAR13(Legacy DMA Controller Master Clear Port)

Legacy Address: DDMASlaveBase + 0Dh || 000Dh

Default Value:

Access: Write Only

BIT	ACCESS	DESCRIPTION
0	WO	master clear register for implemented legacy 8237-A DMA channel . Writing to this register has the effect of hardware reset to the implemented legacy 8237-A DMA channel. Implementation of this register maintains the register compatibility with legacy 8237-A DMA controller for system with or without DDMA Master. For system which has DDMA Master, it is the DMA Master's responsibility to write to this register when a write to legacy 8237-A master clear register (I/O write to 000Dh) is on the PCI Bus. When snooping legacy 8237-A register operation is enabled, any I/O write to 000Dh should clear several legacy flags such as

		First_Last flag.

Register: Eh DMAR14(Legacy DMA Controller Clear Mask Port)

Legacy Address: 000Eh

Default Value:

Access: Write Only

BIT	ACCESS	DESCRIPTION
0	WO	multi-channel mask clear port for implemented legacy 8237-A DMA channel . Writing to this register will affect the legacy DMA operation of TSAudio , implementation of this register maintains the register compatibility with legacy 8237-A DMA multi-channel clear mask register . For system which has DDMA Master, it is the DMA Master's responsibility to update the legacy channel mask bit DMAR15.0 with address (DMASlaveBase + Fh) when a I/O write to 000Eh occurred on PCI Bus. When snooping legacy 8237-A register operation is enabled, any I/O write to 000Eh will reset DMAR15.0 to 0.

Register: Fh DMAR15(Legacy DMA Controller Multi-Channel Mask Register)

Legacy Address: DDMASlaveBase + 0Fh || 000Fh

Default Value: 0b

Access: Write Only

BIT	ACCESS	DESCRIPTION
1	WO	multi-channel mask register for implemented legacy 8237-A DMA channel . Implementation of this register maintains the register compatibility with legacy 8237-A DMA controller for system with or without DDMA Master. For system which has DDMA Master, it is the DMA Master's responsibility to write DMAR15 when a write to legacy 8237-A multi-channel mask register (I/O write to 000Fh) is on the PCI Bus. When snooping legacy 8237-A register operation is enabled, any I/O write to 000Fh should update the mask flag for the implemented legacy 8237-A DMA channel.

Register 10h SBR0 (Legacy FmMusic Bank 0 Register Index / Legacy FmMusic Status)

Legacy Address: SBBase + 0h || SBBase + 8h || ADLIBBase + 0h

Default Value: 00h

Access: Read/Write

BIT	ACCESS	DESCRIPTION

7:0	RW	1:FmMusic Timer Interrupt Flag (Equal to Bit 6 + Bit 5) 1:FmMusic Timer 1 Overflowed Flag 1:FmMusic Timer2 Overflowed Flag 0:Reserved Legacy FmMusic Bank 0 Register Index

Relative Internal Function Register File

Inorder to emulate the legacy FmMusic(YMF262 or OPL3) function, a 512 bytes register file (RAM) must be implemented. By legacy access method, this register file has two banks and the bank index is specified by SBR0 and SBR2 respectively. This register file is byte-wide format , read/write RAM which has no high speed operation requirement.

Relative Internal Functional Register Extracted From Legacy FmMusic Bank 0 Register File

FmMusic-TIMER1

Bank Index : 02h

Size : 8 bits

Type : read/write

Default : 00h

Bit 7..0 X Timer1 Preset Value

If enabled, Timer1 counter will increase every 1024 AC97 bitclock (12.288MHz) . When overflow occurs, this value is re-loaded into the counter.

FmMusic-TIMER2

Bank Index : 03h

Size : 8 bits

Type : read/write

Default : 00h

Bit 7..0 X Timer2 Preset Value

If enabled, Timer2 counter will increase every 4096 AC97 bitclock (12.288MHz). When overflow occurs, this value is re-loaded into the counter.

FmMusic-Timer-CONTROL

Bank Index : 04h

Size : 8 bits

Type : read/write

Default : 00h

Bit 7	1	Reset Bit 7-5 of Legacy FmMusic Status Register
Bit 6	1	Reset Timer1 Overflow Flag
Bit 5	1	Reset Timer2 Overflow Flag
Bit 4-2	0	Reserved
Bit 1	1	Enable Timer 2
Bit 0	1	Enable Timer 1

Bit 7-5 must be self-cleared to 0 after it is written as 1.

When bit 1 or 0 is set from 0 to 1, the corresponding timer counter will load its preset value and start counting. When these bits are zero, the respective timer counter will stop counting. If bit 1 is set 1, bit 7 and 5 of FmMusic Status register will be set 1 when timer2 is overflowed. If bit 0 is set 1, bit 7 and 6 of FmMusic Status register will be set 1 when timer1 is overflowed.

Register: 11h / 13h SBR1 (Legacy FmMusic Bank 0 Register Data Port)

Legacy Address: SBBase + 1h || SBBase + 9h || ADLIBBase + 1h || SBBase + 3h || ADLIBBase + 3h

Default Value: XXh

Access: read/write

BIT	ACCESS	DESCRIPTION
7:0	R/W	Legacy FmMusic Bank 0 Register(indexed by SBR0) Data

When writing to this register, if SBR0 is B0h-B8h and bit 5 of the content (indexed by SBR0) is changed from 0 to 1 or vice versa, or SBR0 is BDh and any one of bit 4-0 of the content (indexed by SBR0) is changed from 0 to 1 or vice versa, an OPL3 Bank0 Key On/Off Dirty Flag will be set at TSAudio Status Register ASR0 and AOPLSR0.

Register: 12h SBR2 (Legacy FmMusic Bank 1 Register Index)

Legacy Address: SBBase + 2h || ADLIBBase + 2h

Default Value: 00h

Access: read/write

BIT	ACCESS	DESCRIPTION
7:0	R/W	Legacy FmMusic Bank 1 Register Index

Register: 11h / 13h SBR3 (Legacy FmMusic Bank 1 Register Data Port)

Legacy Address: SBBase + 1h || ADLIBBase + 1h || SBBase + 3h || ADLIBBase + 3h

Default Value: XXh

Access: read/write

BIT	ACCESS	DESCRIPTION
7:0	R/W	Legacy FmMusic Bank 1 Register(indexed by SBR2) Data

When write to this register, if SBR2 is B0h-B8h and bit 5 of the content (indexed by SBR2) is changed from 0 to 1 or vice versa, an OPL3 Bank1 Key On/Off Dirty Flag will be set at TSAudio Status Register ASR0 and AOPLSR0.

Register: 14h SBR4 (Legacy Sound Blaster Mixer Register Index)

Legacy Address: SBBase + 4h

Default Value: 00h

Access: read/write

BIT	ACCESS	DESCRIPTION
7:0	R/W	Legacy SB16 / SBPRO Mixer Register Index

Register: 15h SBR5 (Legacy Sound Blaster Mixer Register Data Port)

Legacy Address: SBBase + 5h

Default Value: XXh

Access: read/write

BIT	ACCESS	DESCRIPTION
7:0	R/W	Legacy SB16 / SBPRO Mixer Register (indexed by SBR4) Data Port

Register: 16h / 17h SBR6 (Legacy Sound Blaster ESP Reset Port)

Legacy Address: SBBase + 6h || SBBase + 7h

Default Value:

Access: write only

BIT	ACCESS	DESCRIPTION
0	WO	1:Enter Legacy SB16 / SBPRO ESP Reset State 0:Escape From SB16 / SBPRO ESP Reset State

ESP Reset should do the following things:

a. Reset ESP to no operation status and clear ESP Busy Flag.

b. Stop wave engine SB channel operation.

Reset any flags that may affect the next command execution.

Register: 1Ah / 1Bh SBR7 (Legacy Sound Blaster ESP Data Port)

Legacy Address: SBBase + Ah || SBBase + Bh

Default Value: 00h

Access: Read only

BIT	ACCESS	DESCRIPTION
7:0	RO	Data returned by Legacy SB16 / SBPRO ESP Read Operation

Register: 1Ch / 1Dh SBR8 (Legacy Sound Blaster Command / Status Port)

Legacy Address: SBBase + Ch || SBBase + Dh

Default Value: 00h

Access: read/write

BIT	ACCESS	DESCRIPTION
7:0	WO	The Command (Operator) or Data (Operand) Written to Legacy SB ESP
7	RO	0:Legacy SB ESP is Available For Next Command / Data 1:Legacy SB ESP is Busy.
6:0	RO	**Reserved**

After the command / data has been written to the ESP Command / DATA port, bit 7 of this status register will be set to 1 (busy) . After ESP has processed the written command / data and waiting for the next one , bit 7 of this status register will be reset to 0 (not busy). Any acknowledge byte must be readback before any new command is issued. ESP will be set busy after this port has ever been written and will be set not busy if the command/status has been read four times.

Register: 1Eh SBR9 (Legacy Sound Blaster ESP Data Ready / IRQ Acknowledge Port 1)

Legacy Address: SBBase + Eh

Default Value: 00h

Access: read only

BIT	ACCESS	DESCRIPTION
7	RO	0:Data is not available on SBR7. 1:Data is available on SBR7.

6:0	RO	**Reserved**

Reading this register will clear the interrupt generated by the ESP for NON-BX type legacy SB DMA command.

After SBR7 has been read, bit 7 of this register will reset to 0 (no data) until the next read data is available and set bit 7 of this register.

Register: 1Fh SBR10 (Legacy Sound Blaster ESP Data Ready / IRQ Acknowledge Port 2

Legacy Address: SBBase + Fh

Default Value: 00h

Access: Read only

BIT	ACCESS	DESCRIPTION
7	RO	0:Data is not available on SBR7. 1:Data is available on SBR7.
6:0	RO	**Reserved**

Reading this register will clear the interrupt generated by the ESP for BX type legacy SB DMA command.

After SBR7 has been read, bit 7 of this register will reset to 0 (no data) . If the next read data is available at SBR7, bit 7 of this register will again be set to 1.

Register: 20h MPUR0 (Legacy MPU-401 Data Port / IRQ Acknowledge Port)

Legacy Address: MPU401Base + 0h

Default Value: FEh

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7:0	R/W	MPU-401 Acknowledge Byte or External MIDI Input Data in MIDI-IN FIFO MIDI Output Data

When internal loopback mode is enabled, reading this port will not update the MIDI-IN FIFO read counter.

Register: 21h MPUR1 (Legacy MPU-401 Command / Status Port)

Legacy Address: MPU401Base + 1h

Default Value: 80h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	0:Ack. Byte is available or External MIDI Input Data is Available

		in MIDI-IN FIFO; 1:NO Acknowledge Byte or External MIDI Input Data;
6	R/W	0:Ready for MIDI Data Output or New MIDI Command 1:MIDI-OUT FIFO is Full
5	R/W	0:MIDI-IN FIFO is not Full 1:MIDI-IN FIFO is Full
4	R/W	0:MPU401 engine is at PASS-THRU mode 1:MPU401 engine is at UART mode
3:0	R/W	**Reserved** Command to MPU-401 MIDI Controller;

Register: 22h MPUR2 (MPU-401 Operation Control / Status Register)

Legacy Address: MPU401Base + 2h

Default Value: 10h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	0:MIDI-IN FIFO Source From External MIDI-IN Pad; MIDI-IN FIFO Source From MIDI-OUT FIFO; 1:MIDI-IN FIFO Source From MIDI-OUT FIFO;OUT FIFO;
6	R/W	0:External MIDI-OUT Pad Source From MIDI-OUT FIFO; 1:External MIDI-OUT Pad Source From External MIDI-In Pad; 0:External MIDI-OUT Pad Source From MIDI-OUT FIFO; 1:External MIDI-OUT Pad Source From External MIDI-In Pad;
5	R/W	0:Regualr MIDI Clock is being used ; Fast MIDI Clock (12.288MHz) is being used; 0:Regualr MPU401 MIDI Clock is being used ; 1:Fast MPU401 MIDI Clock (12.288MHz) is being used
4	R/W	0:MPUR0 Disconnect From MIDI-OUT FIFO; 1:Connect MPUR0 to MIDI-OUT FIFO; 0:Disconnect MPUR0 From MIDI-OUT FIFO When at Pass-Thru Mode; 1:Connect MPUR0 to MIDI-OUT FIFO When at Pass-Thru Mode;

3	R/W	0:Interrupt will be generated When MIDI-IN FIFO is not Empty; Interrupt will not be gererated When MIDI-IN FIFO is not Empty; 0:Generate Interrupt When MIDI-IN FIFO is not Empty; 1:Do Not Generate Interrupt When MIDI-IN FIFO is not Empty
2	R/W	0:MPU401 Midi-out buffer full flag is not masked at loop back mode; MPU401 Midi-out buffer full flag is masked at loop back mode; 0:External midi-out source from internal midi-out 1:Force external midi-out output pad to stay at high level
1	R/W	0:MIDI-OUT FIFO is Empty; MIDI-OUT FIFO is Not Empty; **Reserved**
0	R/W	0:MIDI-IN FIFO is Empty; 1:MIDI-IN FIFO is not Empty; **Reserved**

Register: 23h MPUR3 (MPU-401 MIDI-IN FIFO Access Port)

Legacy Address: MPU401Base + 3h

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	MIDI Data Serialized In MIDI-IN FIFO

After power up reset , MPU-401 MIDI engine is at pass-through mode.

MPU-401 MIDI engine will only execute the following two commands when at pass-through mode.

Command Code : 3Fh

Function : Enter_UART Mode From Pass-Through Mode

Behavior : Return acknowledge byte (0FEh) in MPUR0, generate an interrupt if switch to UART mode successfully. Reading MPUR0 will clear this interrupt.

Command Code : FFh

Function : MIDI Reset

Behavior : Return acknowledge byte (0FEh) in MPUR0, generate an interrupt and stay in Pass-Through mode. Reading MPUR0 will clear this interrupt.

MPU-401 MIDI engine will only execute the following command when at UART mode.

Command Code : FFh

Function : Enter Pass-Through Mode From UART Mode

Behavior : Flush MIDI-IN FIFO, go to Pass-Through mode;

When MPU-401 MIDI engine is at internal loopback operation state (MPUR3.7 is set 1), MPUR1.7 is masked from MIDI-IN FIFO state automatically. This means if MIDI-IN FIFO is not empty, MPUR1.7 is still reading as 1. When MIDI-IN FIFO is full, MIDI clock will be stopped until MIDI-IN FIFO is not full.

Register: 30h GAMER0 (Gameport Control Register)

Legacy Address:

Default Value: 0h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
7	R/W	0:Disable Enhanced Digital Gameport; 1:Enable Enhanced Digital Gameport
6	R/W	0:Disable Testmode for Enhanced Mode Gameport Enable Testmode for Enhanced Mode Gameport
5:0	R/W	**Reserved**

When Bit6 is set, the gamecounter will overflow every 1024 AC97 Bitclk. Bit 6 is only useful when Bit 7 is set.

Bit 7 will be automatically cleared if there are any I/O operation to GAMER1.

Register: 31h GAMER1 (Legacy Gameport I/O Register)

Legacy Address: GAMEBase + 0 - 7h

Default Value: 00h

Access: Read/Wrie

BIT	ACCESS	DESCRIPTION
7:0	W	Trigger the Legacy Gameport I/O Read Cycle
7	R	0:Joystick B Button1 Pressed (Input Pad Stay At Low Level) 1:Joystick B Button1 Released(Input Pad Stay At High Level)
6	R	0:Joystick B Button0 Pressed(Input Pad Stay At Low Level)

		1:Joystick B Button0 Released(Input Pad Stay At High Level)
5	R	0:Joystick A Button1 Pressed(Input Pad Stay At Low Level) 1:Joystick A Button1 Released(Input Pad Stay At High Level)
4	R	0:Joystick A Button0 Pressed(Input Pad Stay At Low Level) 1:Joystick A Button0 Released(Input Pad Stay At High Level)
3	R	0:Joystick B Y-Axies Input Pad Stay at High Level 1:Joystick B Y-Axies Input Pad Stay at Low Level
2	R	0:Joystick B X-Axies Input Pad Stay at High Level 1:Joystick B X-Axies Input Pad Stay at Low Level
1	R	0:Joystick A Y-Axies Input Pad Stay at High Level 1:Joystick A Y-Axies Input Pad Stay at Low Level
0	R	0:Joystick A X-Axies Input Pad Stay at High Level 1:Joystick A X-Axies Input Pad Stay at Low Level

Register 34h GAMER2 (Enhanced Gameport Position Register 1)

Legacy Address:

Default Value: 00000000h

Access: Read Only

BIT	ACCESS	DESCRIPTION
31:16	R/W	Joystick A Y-Axies Position Latch Value (16 bit unsigned)
15:0	R/W	Joystick A X-Axies Position Latch Value (16 bit unsigned)

Register 38h GAMER3 (Enhanced Gameport Position Register 2)

Legacy Address: AudioBase + 38h

Default Value: 00000000h

Access: Read Only

BIT	ACCESS	DESCRIPTION
31:16	RO	Joystick B Y-Axies Position Latch Value (16 bit unsigned)
15:0	RO	Joystick B X-Axies Position Latch Value (16 bit unsigned)

Any I/O operation to legacy GAMEBase will function as normal gameport mode.

At enhanced gameport mode (GAMER0.7 is set 1), when the 16 bit game counter overflowed, the external pad for joystick A&B X-Y Axies State will stop drived low, then game counter will counting up from zero with AC97 bitclock (12.288 MHz). Each game position

latch (4 * 16 bits) will store the game counter value when its corresponding axies state pad recharged from low to high. When the game counter overflowed, the game position latch will be set to the overflowed value (0FFFFh) if its corresponding axies state pad is still low.

The game position latches can be read in word or double word format. These latches should be frozen when reading and be freed after reading.

Register 40h ACWR(AC-97 Mixer Write Register)

Legacy Address:

Default Value: : 00000000h

Access: Read /Write

BIT	ACCESS	DESCRIPTION
31:16	R/W	data to be written into AC-97 mixer register. data to be written into AC-97 mixer register;
15	R/W	0:ready to write AC-97 mixer register 1:busy writing AC-97 mixer (indexed by Bit 7..0); 0:do nothing 1:write AC-97 mixer register (indexed by bit 7..0) with bit 31..16;
14:7	R/W	**Reserved**
6:0	R/W	index of the AC-97 mixer register to be written; index of the AC-97 mixer register to be written; Bit 7=0 for Primary CODEC; Bit 7=1 for Secondary CODEC.

Register 44h ACRD(AC-97 Mixer Read Register)

Legacy Address:

Default Value: 00000000h

Access: Read /Write

BIT	ACCESS	DESCRIPTION
31:16	R/W	AC-97 mixer register contents **Reserved**
15	R/W	0:bit 31..16 is valid data of AC-97 mixer register (indexed by bit 7..0) 1:busy reading AC-97 mixer register (indexed by bit 7..0); 0:do nothing

		1:read AC-97 mixer register (indexed by bit 7..0) to bit 31..16;
14:7	R/W	**Reserved**
6:0	R/W	index of the AC-97 mixer register to be read; index of the AC-97 mixer register to be read; Bit 7=0 for Primary CODEC; Bit 7=1 for Secondary CODEC.

Register 48h SCTRL (Serial INTF Control Register)

Legacy Address:

Default Value: 00014000h

Access: Read /Write

BIT	ACCESS	DESCRIPTION
26	RO	CODEC Power Down State flag 0:Normal 1: CODEC is in power down mode When PM_ST enters D3, this bit will be set.
25	RO	Secondary CODEC Ready flag 0: Not ready 1: Ready
24	RO	Primary CODEC Ready flag 0: Not ready 1: Ready
23	R/W	GPIOOUT Slot Enable 0: Disable 1: Enable (If DBLRATE_EN is 0)
22	R/W	HSETOUT Slot Enable 0: Disable 1: Enable (If DBLRATE_EN is 0)
21	R/W	LINE2OUT Slot Enable 0: Disable 1: Enable (If DBLRATE_EN is 0)
20	R/W	LINE1OUT Slot Enable

		0: Disable 1: Enable
19	R/W	LFEOUT Slot Enable 0: Disable 1: Enable
18	R/W	CENTEROUT Slot Enable 0: Disable 1: Enable
17	R/W	SURROUT L/R Slot Enable 0: Disable 1: Enable
16	R/W	PCMOUT L/R Slot Enable, Default: 1 0: Disable 1: Enable (Default)
15:14	R/W	Secondary CODEC ID Default: 01
13	R/W	GPIOIN Slot Select 0: Primary CODEC GPIOIN slot input to GPIOIN buffer 1: Secondary CODEC GPIOIN slot input to GPIOIN buffer
12	R/W	HSETIN Slot Select 0: Primary CODEC HSETIN slot input to HSETIN buffer 1: Secondary CODEC HSETIN slot input to HSETIN buffer
11	R/W	LINE2IN Slot Select 0: Primary CODEC LINE2IN slot input to LINE2IN buffer 1: Secondary CODEC LINE2IN slot input to LINE2IN buffer
10	R/W	MIC Slot Select 0: Primary CODEC MIC slot input to MIC buffer 1: Secondary CODEC MIC slot input to MIC buffer
9	R/W	LINE1IN Slot Select 0: Primary CODEC LINE1IN slot input to LINE1IN buffer 1: Secondary CODEC LINE1IN slot input to LINE1IN buffer

8	R/W	PCMIN Slot Select 0: Primary CODEC PCMIN slot input to PCMIN_A buffer 1: Secondary CODEC PCMIN slot input to PCMIN_A buffer
7	R/W	I2S Input Function Enable 0: Disable If disabled, the clocks of I2S receiver should be shut down. 1: Enable
6	R/W	I2S Output Function Enable 0: Disable If disabled, the clocks of I2S transmitter should be shut down. 1: Enable
5	R/W	S/PDIF Output Function Enable 0:Disable If disabled, the clocks of SPDIF transmitter should be shut down. 1: Enable
4	R/W	CODEC Double Rate Enable 0: Disable 1: Enable
3	R/W	PCM Output Select (Primary/Secondary) 0: PCM Output up to Primary CODEC request 1: PCM Output up to Secondary CODEC request
2	R/W	MCLK clock rate select for I2S Output 0: MCLK = 12.288M 1: MCLK = 6.144M
1	R/W	CODEC Cold Reset Command 0: Normal 1: Cold Reset CODEC When write '1' to this bit, pin ACRST# should be driven to low for at least 1us.
0	R/W	CODEC Warm Reset Command 0: Normal 1: Warm Reset CODEC

		When write '1' to this bit, pin ACSYNC should be driven to high for at least 1us.

Register 4ch ACGPIO (AC97 General Purpose IO Register)

Legacy Address:

Default Value: 00000000h

Access: Read /Write

BIT	ACCESS	DESCRIPTION
31:16	R/W	data to be written into AC-97 through output Slot 12;
15	R/W	This bit is status when read. 0:ready to output AC-97 Slot 12 1:busy This bit is command when write 0:do nothing 1:output AC-97 Slot 12
14:5	R/W	reserved
4	R/W	Secondary CODEC GPIO_INT Enable 0:Disable 1:Enable
3	R/W	Primary CODEC GPIO_INT Enable 0:Disable 1:Enable
2	R/W	Secondary CODEC GPIO_INT register This bit will be updated with Secondary input Slot 12 bit 0 of every AC97 frame.
1	R/W	Primary CODEC GPIO_INT register This bit will be updated with Primary input Slot 12 bit 0 of every AC97 frame.
0	R/W	**Reserved**

Register 50h ASR0 (TSAudio Status Register)

Legacy Address:

Default Value: 00000000h

Access: Read Only

BIT	ACCESS	DESCRIPTION
31:30	RO	Reserved
29	RO	Read/Write, MPU401 Output Buffer Select 0: 8-byte 1: 128-byte
28	RO	Legacy Recording IRQ MASK 0:Generate IRQ when legacy recording block length expired. 1:Don't generate IRQ when legacy recording block length expired
27	RO	1:SB ESP is at special DMA mode
26:25	RO	00:SB ESP is at get operator state 01:SB ESP is at get first operand state 11:SB ESP is at get second operand state 10:SB ESP is at get third operand state
24	RO	1:SB Mixer Soft-Reset
23	RO	1:SB PRO Command Captured Most Recently (Non-Bx or Cx Type Command Captured)
22	RO	1:SB16 Command Captured Most Recently (Bx or Cx Type Command Captured)
21	RO	1:SB Engine Sample Rate Set By Frequency Most Recently
20	RO	1:SB Engine Sample Rate Set By Time Constant Most Recently
19	RO	1:SB16 Mixer Register Update
18	RO	1:SB PRO Mixer Register Update
17	RO	1:OPL3 Bank1 Key On/Off
16	RO	1:OPL3 Bank0 Key On/Off
15	RO	0:AC-97 codec is not ready 1:AC-97 codec is ready
14	RO	0:SB Mixer Register MX0E.1 is 0 1:SB Mixer Register MX0E.1 is 1
13	RO	0:SB ESP is not at Direct Recording Mode 1:SB ESP is at Direct Recording Mode
12	RO	0:SB ESP has no ack byte

		1:SB ESP has ack byte that needs to be read out
11	RO	0:SB ESP DMA Command is not valid 1:SB ESP DMA command is valid
10	RO	0:SB ESP Engine at Digital Audio Off State 1:SB ESP Engine at Digital Audio On State
9:8	RO	00:SB ESP Engine Command Port Not Busy 01:SB ESP Engine Command Port Busy 10:SB ESP DMA Test Busy 11:SB ESP Command Buffer Full
7	RO	0:8 bit data format 1:16 bit data format
6	RO	0:mono 1:stereo
5	RO	0:unsigned data format 1:signed data format
4	RO	0:playback 1:recording
3	RO	0:SB DMA loop disable 1:SB DMA loop enable
2:0	RO	LegacyCMD 000 stop : No any operation. No contribution to Digital Mixer 001 run : Normal operation. 010 silent_DMA : SBCL will count; CA, CBC won't count. No data fetching. No interpolation. No contribution to Digital Mixer 011 reserve 100 silent_SB : SBCL, CA & CBC will count as the same as run mode.No data fetching. No interpolation. No contribution to Digital Mixer 101 pause : SBCL, CA & CBC don't change. let SBALPHA unchanged, CACHE_HIT=1 drive current LD (or LD_L, LD_R) to Digital Mixer

		110 reserve 111 direct play : SBCL, CA & CBC don't change. drive SBDD to Digital Mixer

Only one bit of Bit 21 and Bit 20 can be set 1 by implemented SB ESP Engine at any time.

Only one bit of Bit 23 and Bit 22 can be set 1 by implemented SB ESP Engine at any time.

Register 54h ASR1 (Legacy Sound Blaster Frequency Read Back Register)

Legacy Address: AudioBase

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
15:0	RO	Sample Frequency Set by SB Command 41h or 42h

Register 56h ASR2 (Legacy Sound Blaster Time Constant Read Back Register)

Legacy Address: AudioBase

Default Value: 00h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	Time Constant Value Set by SB Command 40h

Register 58h ASR3 (TSAudio Scratch Register)

Legacy Address:

Default Value: 00000000h

Access: Read / Write

BIT	ACCESS	DESCRIPTION
31:0	R/W	

Register 5ch ASR4 (TSAudio Version Control Register)

Legacy Address:

Default Value: 80h

Access: Read Only

BIT	ACCESS	DESCRIPTION
7:0	RO	

Register 5Eh ASR5 (SB ESP Version High Byte Control Register)

Legacy Address:

Default Value: 4h

Access: Read /Write

BIT	ACCESS	DESCRIPTION
3:0	R/W	

Register 5Fh ASR6 (SB ESP Version Low Byte Control Register)

Legacy Address:

Default Value: 2h

Access: Read / Write

BIT	ACCESS	DESCRIPTION
3:0	R/W	

Register 60h AOPLSR0 (OPL3 Emulation Channel Keyon/off Trace Register)

Legacy Address:

Default Value: 00000000h

Access: Read Only

BIT	ACCESS	DESCRIPTION
31:25	RO	Reserved
24:16	RO	Bank1 channel 8-0 key on/off event captured
15	RO	Read only 0:Bank0 1:Bank1
14	RO	Reserved
13:9	RO	1:OPL3 rhythm channel 4-0 key on/off event captured
8:0	RO	1:Bank0 channel 8- 0 key on/off event captured.

All the flag will be cleared after this register is read.

Register 70h SPDIF_CS (S/PDIF Channel Status Register)

Legacy Address:

Default Value: 02000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:30	R/W	Reserved Hardwired to 00b
29:28	R/W	Clock Accuracy

		Read/Write, Default: 00b
27:24	R/W	Sample rate Read/Write, Default: 2h (48kHz)
23:20	R/W	Read/Write, Default: 0h
19:16	R/W	Read/Write, Default: 0h
15:8	R/W	Read/Write, Default: 00h
7:6	R/W	Read/Write, Default: 00b
5:3	R/W	Read/Write, Default: 000b
2	R/W	Copyright Read/Write, Default: 00b
1	R/W	Audio content flag Read/Write, Default: 0
0	R/W	Professional flag Read/Write, Default: 0

Register 74h New_Sub_ID (New Sub-system ID & Sub-vendor ID)

Legacy Address:

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:16	R/W	The new Sub-system ID in this word will be loaded into external EEPROM during EEPROM writing phase;
15:0	R/W	The new Sub-vendor ID in this word will be loaded into external EEPROM during EEPROM writing phase.

Register 78h EEPROM_CTRL (EEPROM interface control register)

Legacy Address:

Default Value: 08000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31	R/W	Read only, active high. 0:EEPROM interface controller is idle. PCI configuration read 2Ch will return stable value, and BIOS can issue a EEPROM write command; 1:EEPROM interface controller is busy, i.e. it's either in reading

		phase or in writing phase. PCI configuration read 2Ch will be re-tried by audio chip, and BIOS can not issue a EEPROM write command;
30	R/W	Read only, active high. Write '1' to clear. 0:Normal, EEPROM writing phase is completed successfully; 1:EEPROM configration failed. After EEPROM writing phase is completed, controller will automatically read data back. If result doesn't match or there's error in reading phase, this bit will be set.
29	R/W	Read only, active high. Write '1' to clear. 0:Normal, EEPROM reading phase is completed successfully, i.e. data complementary rule checking is OK. This bit will be reset to '0' at the beginning of an EEPROM writing phase. 1:EEPROM reading failed, i.e. data complementary rule checking failed. Data complementary rule: In external EEPROM, word0 is Sub-vendor ID, word1 is 1's complement of word0; Word2 is Sub-system ID, word3 is 1's complement of word2;
28	R/W	Read only, active high. Write '1' to clear. 0:Normal. 1:EEPROM absence flag. This bit will be set to '1' when each bit of data read in is '1'.
27	R/W	Read/Write, active high. 0:Disable. 1:Enable. (Default)
26	R/W	Read/Write, active high. EEPROM Write command. 0:Normal. 1:Write '1' to start EEPROM Write. When write phase complete, this bit will be reset to '0'.
25	R/W	Read/Write, active high. EEPROM interface test mode enable bit. 0:Normal mode. 1:Test mode. EEPROM interface will run 8x faster than normal
23:22	R/W	Read/Write, OP-code of EEPROM controller 00:Null 01:Read

		10:Write 11:Reserved
21:16	R/W	Read/Write, Address of EEPROM
15:0	R/W	Read only.

Register 7Ch GPIO(General purpose IO Register)

Legacy Address:

Default Value: 00000000h

Access: Read /Write

BIT	ACCESS	DESCRIPTION
31:24	R/W	reserved
23:16	R/W	GPControl[7:0] 0:Input GPI[7:0] = GP_PIN[7:0] 1:Output GP_PIN[7:0] = GPO[7:0]
15:8	R/W	GPO[7:0]
7:0	R/W	GPI[7:0]

All reserved bits return 0 when read.

8.16.1 WAVE ENGINE REGISTER:

64 voice channels are classified into two banks.
Bank A: channel 0-31 (optimized for MIDI)

Bank B: channel 32-63 (optimized for Wave, WDM Stream, DirectX buffer, I^2S, S/PDIF, MODEM, Handset, Recording, Microphone, Main Mixer Capture, Reverb Send, Chorus Send, AC97 SURR, AC97 CENTER/LFE)

Each channel in Bank A can only be programmed as a playback channel with individual EM(envelope modulation), individual LFO AM and individual LFO FM.

Channels in Bank B have more flexibility. Each of them can be programmed as a Normal PB channel with global LFO AM and LFO FM but without EM, or as a Special PB channel, or as a REC channel, or as a REC_PB channel. Bit[31:19] of RegEC_B is Channel ATTRIBUTE.

Register 80h STAR_A (START command and status register for Bank A)

Legacy Address:

Default Value: 00000000h

Access: Read / Write

BIT	ACCESS	DESCRIPTION

31:0	R/W	This register and STOP_A are used as Bank A channel start/stop command register when they are written, and used as Bank A channel running/stopped status register when they are read. bit n is for channel n. Reading from this I/O port will return the running/stopped status of Bank A 32 voice channels. 0:Stopped. When bit n is read as '0', it means any operation of channel n, including address generation, sample data fetching, interpolation, and envelope calculation is stopped. And this channel has no contribution to the digital mixer. This bit will be reset from '1' to '0' in four cases. (1) when a '1' is written to the corresponding bit in register STOP_A . (2) when out of data, i.e. when sample loop disabled and CSO (Current Sample Offset) >= ESO (End Sample Offset). (3) when Ec (current envelope) drops down to -63.984375 dB. (4) when current envelope buffer is in delay-stop mode, and EDLY count down to '0'. 1:Running. When bit n is read as '1', it means channel n is working. This bit will be set from '0' to '1' only when a '1' is written to the corresponding bit in register START_A. Writing to this I/O port means issuing a start command to address engine and envelope engine in expected channel. 0:Ignore. A '0' written to bit n will not change the status of channel n. 1:Start. A '1' written to bit n will start channel n's address engine and envelope engine and also set the status bit n to '1'.

Register 84h STOP_A (Channel STOP command and status register for Bank A)

Legacy Address:

Default Value: 00000000h

Access: Read / Write

BIT	ACCESS	DESCRIPTION
31:0	R/W	Reading from this I/O port will return the same value as from the

		last register START_A. Writing to this I/O port means issuing a stop command to address engine and envelope engine in expected channel. 0:Ignore. A '0' written to bit n will not change the status of channel n. 1:Stop. A '1' written to bit n will stop channel n's address engine and envelope engine, and also reset the corresponding status bit to '0'.

Register 88h DLY (Delay flag of Bank A)

Legacy Address:

Default Value: 00000000h

Access: Read / Write

BIT	ACCESS	DESCRIPTION
31:0	R/W	When read, this register will show the delay status of each channel of Bank A. Bit n is for channel n. 0:normal This bit will toggle from '1' to '0' when envelope engine change from a delay mode buffer to a non-delay mode buffer. When channel n is stopped, bit n will be reset to '0'. 1:channel is currently in delay mode (address engine keep stopped but envelope engine is running). This bit will toggle from '0' to '1' only when envelope engine begin to deal with a delay mode buffer. When write, 0:ignore (don't change) 1:set to '1'

Register 8Ch SIGN_CSO (Sign bit of CSO) (for Bank A only)

Legacy Address:

Default Value: 00000000h

Access: Read / Write

BIT	ACCESS	DESCRIPTION
31:0	R/W	This register is used to store the sign bits of 32 channel's CSO of Bank A, with '0' means current sample address is greater than or

		equal to LBA(Loop Begin Address), while '1' means current sample address is little than or equal to LBA. This register can be programmed with an initial status and will be updated by address engine. Write '0':ignore (don't change) Write '1':set to '1' When channel n is stopped, bit n will be reset to '0'.

Register 90h CSPF_A(Bank A Current Sample Position Flag)

Legacy Address:

Default Value: 00000000h

Access: Read only

BIT	ACCESS	DESCRIPTION
31:0	RO	This register will show a flag which indicates the Bank A's current sample is in a range between ESO/2 to ESO or in a range before ESO/2 (ESO is offset from loop begin to loop end). And this flag will be used for sample data double buffering control. Bit n is for channel n. 0:Before ESO/2 1:From ESO/2 to ESO When channel n is stopped, bit n will be reset to '0'.

Register 94h CEBC (Current Envelope Buffer Control) (for Bank A only)

Legacy Address:

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:0	R/W	Reading from this register will return current envelope buffer flags of 32 channels of Bank A, which indicate currently envelope engine is using parameters from EBUF1 or EBUF2. Bit n is for channel n. 0:Buffer 1 1:Buffer 2 Writing '1' to bit n of this register will toggle the flag in channel n and force envelope engine to change buffer. Writing '0' to bit n won't change anything in channel. 0:Ignore 1:Toggle

		When channel n is stopped, bit n will be reset to '0'.

Register 98h AINT_A (Bank A address engine interrupt)

Legacy Address:

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:0	R/W	Any bits toggled from '0' to '1' will result in a IRQ. Reading from this I/O port will return the address INT status of Bank A's 32 channels. Bit n is for channel n. 0:No INT 1:INT This bit will be set in 2 cases: When CSO (current sample offset) >= ESO (end sample offset), and ENDLP_IE (end of loop INT enable bit in Global Control register) =1 and AINTEN_A bit n is set 1 For channel n. When CSO (current sample offset) >= ESO/2 (middle of ESO), and MIDLP_IE (middle of loop INT enable bit in Global Control register) =1 and AINTEN_A bit n is set 1 for channel n. Writing '1' to bit n of this register will reset this bit. 0:Ignore. A '0' written to bit n will not change the status of this bit. 1:reset A '1' written to bit n will reset this bit.

Register 9Ch EINT(Envelope engine interrupt register) (for Bank A only)

Legacy Address:

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:0	R/W	Any bits toggled from '0' to '1' will result in a IRQ. Reading from this I/O port will return the envelope INT status of 32 channels of Bank A. Bit n is for channel n. 0:No INT 1:INT

		This bit will be set in 2 cases: When envelope buffer toggled, and ETOG_IE (envelope toggle INT enable bit in Global Control register) =1. When Ec (current envelope) <= FFFh (-63.984375 dB), and EDROP_IE (envelope dropping to -63.984375dB INT enable bit in Global Control register) =1. Writing '1' to bit n of this register will reset this bit. 0:Ignore. A '0' written to bit n will not change the status of this bit. 1: reset A '1' written to bit n will reset this bit.

Register A0h GC & CIR (Global Control & Channel Index)

Legacy Address:

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:30	R/W	are used to control Legacy Recording channel when record to mono sample. 00:left 01:right 10: (left+right+1)/2 11: Reserved.

29:28	R/W	Are IO 0008-read handling control bits.
		00:never assert StatusRDY
		01:StatusRDY = DMATCReached
		10:StatusRDY = DMATCReached | LegacyDRQ
		11:in this case, handshaking with StatusWR and manipulation of return byte should been done.
		StatusRDY keep '0' when initialization.
		If(StatusWR ==1) {
		StatusRDY = 1;
		if(DMAChannel==0) {
		ReturnByte[7:0] =
		{InputByte[7:5], DMAR8[4], InputByte[3:1], DMAR8[0]};
		}

		else {
		ReturnByte[7:0] =
		{InputByte[7:6], DMAR8[5], InputByte[4],
		InputByte[3:2], DMAR8[1], InputByte[0]};
		}
		}
		if(DMASNOOPCS_==0 & ADR[7:0] = 8 & Data_rdy_ == 0 & StatusRDY==1)
		StatusRDY = 0;

27	R/W	Test_loopback: This bit is used for wave engine loopback testing. 0:normal 1:force recording engine get new data from playback FIFO instead of aclink.
26	R/W	Debugging Mode 0:Normal 1:Chip is in Debugging Mode. In Debugging Mode, 20 pins (including 8 pins of GPIO, 1 pin of SPDIF , 6 pins of I2S and 5 NC pins) are used as output to monitor 40 internal important signals. Detail in Appendix B.
25:24	R/W	EXPROM Map Mode 00: 000h-1FFh of EXPROM is mapped to AudioMemBase 800h-FFFh low 16 bits; 800h-9FFh of EXPROM is mapped to AudioMemBase 800h-FFFh high 16 bits; 01: 200h-3FFh of EXPROM is mapped to AudioMemBase 800h-FFFh low 16 bits; A00h-BFFh of EXPROM is mapped to AudioMemBase 800h-FFFh high 16 bits; 10: 400h-5FFh of EXPROM is mapped to AudioMemBase 800h-FFFh low 16 bits; C00h-DFFh of EXPROM is mapped to AudioMemBase 800h-FFFh high 16 bits; 11: 600h-7FFh of EXPROM is mapped to AudioMemBase 800h-FFFh low 16 bits; E00h-FFFh of EXPROM is mapped to AudioMemBase 800h-FFFh high 16 bits.

23	R/W	EXPROM Dump Mode Enable 0:Disable 1:Enable If enabled, EXPROM(4096x12bit) is mapped to AudioMemBase according to bit[25:24], i.e. the content of EXPROM can be read out through AudioMem Read cycle.
22:21	R/W	Test mode bits 00:normal mode (chip works normally in this mode) 01:test mode 1 10:test mode 2 11:test mode 3 The detail descriptions on test mode 1, 2, and 3 are given in Appendix B.
20	R/W	Main Mixer Output Control 0:Main Mixer L/R → PCM L/R Output FIFO 1:Main Mixer L/R → MMC L/R Output Buffer
19	R/W	S/PDIF Out Control 0 S/PDIF L/R Output Buffer → S/PDIF L/R transmitter 1:PCM L/R Output FIFO → S/PDIF L/R transmitter
18	R/W	I2S Out Control 0:I2S L/R Output Buffer → I2S transmitter 1:SURR L/R Output FIFO → I2S transmitter
17	R/W	PCMIN_B Mixing Enable/Disable 0:PCMIN_B Mixing Disable 1:PCMIN_B Mixing Enable Note: Controlled by PCMIN_SEL in Reg48h, either of Primary CODEC PCMIN slot or Secondary CODEC PCMIN slot will come into 3-level PCMIN_A buffer. And if PCMIN_B Mixing bit is enabled, the other slot will come into 1-level PCMIN_B buffer and will be mixed into Main Mixer.
16	R/W	64-Channel Mode 0:Legacy Mode 1:64 Channel Mode
15	R/W	is INT enable bit for current envelope dropping to -63.984375dB.

		0:disable 1:enable
14	R/W	is INT enable bit for envelope buffer toggling. 0:disable 1:enable
13	R/W	is INT enable bit for middle of loop. 0:disable 1:enable
12	R/W	is INT enable bit for end of loop. 0:disable 1:enable
11	R/W	is INT enable bit for playback underrun. 0:disable 1:enable When playback FIFO is empty, if this bit is set as '1', a IRQ will be issued.
10	R/W	is INT enable bit for recording overrun. 0:disable 1:enable When recording FIFO is full, if this bit is set as '1', a IRQ will be issued.
9	R/W	is Pause/Resume command bit. Read 0:Engine hasn't been paused yet. 1:Engine has been paused already. Write 0:Resume Engine. 1:Pause Engine. When host writes '1', this bit may not show '1' immediately. Engine will try to get paused as soon as possible. After engine has been paused already, this bit will be set to '1'. Once host writes '0', this bit will be reset to '0' immediately and engine will work normally.
8	R/W	is used to reset playback sample timer counter. When read , return 0;write 1 will reset STimer.
5:0	R/W	is the channel index which is used to select a channel for access. 00h selects channel 0, 1Fh selects channel 31, 3Fh selects

		channel 63.

All other bits are reserved.

Register A4h AINTEN_A(Bank A Address Engine Interrupt Enable)

Legacy Address:

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:0	R/W	This register will control address engine interrupt for each channel of Bank A. Bit n is for channel n. 0:disable address engine interrupt for channel n 1:enable address engine interrupt for channel n

Register A8h MUSICVOL & WAVEVOL(Global Music Volume & Global Wave Volume)

Legacy Address:

Default Value: 00008080h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:24	R/W	music right volume 0 0dB(no attenuation) FFh -63.75dB(mute)
23:16	R/W	music left volume 0 0dB(no attenuation) FFh -63.75dB(mute)
15:8	R/W	wave right volume 0 0dB(no attenuation) 80h -32dB (default) FFh -63.75dB(mute)
7:0	R/W	wave left volume 0 0dB(no attenuation) 80h -32dB (default) FFh -63.75dB(mute)

Register Ach SBDELTA/DELTA_R (Sample Change Step for Legacy Playback & Recording)

Legacy Address:

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:16	R/W	**Reserved.**
15:0	R/W	SBDELTA: Fs/F48k in 4.12 format. SBDELTA_R: F48k/Fs in 4.12 format.

Register B0h MISCINT (Miscellaneous Int & Status)

Legacy Address:

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
24	R/W	(ACGPIO_IRQ) is AC97 GPIO interrupt request. ACGPIO_IRQ = Reg4Ch[1] & Reg4Ch[3] | Reg4Ch[2] & Reg4Ch[4].
23	R/W	(ST_IRQ_En) is ST IRQ enable bit. 0:disable 1:enable
17	R/W	(opltimer_ie) is OPL3 timer interrupt enable bit. 0:disable 1:enable
16	R/W	(PB_24K_MODE) is playback 48k/24k mode control bit. 0:(default)Wave engine drives sample to CODEC at 48Khz 1:Wave engine drives sample to CODEC at 24Khz(in this mode, Delta should be programmed twice as that in 48Khz mode).
15	R/W	(ST_TARGET_REACHED) is a flag with '1' indicates STIMER counter has been equal to ST_TARGET. This bit will be set to '1' once STIMER counter is equal to ST_TARGET. Write '1' will clear this bit.
11	R/W	(mixer_overflow_flag) is a flag which indicates the result of mixer accumulator exceeds 7FFFFh. This bit will be set to '1' once accumulator overflows. Write '1' will clear this bit.

10	R/W	(mixer_underflow_flag) is a flag which indicates the result of mixer accumulator is less than 80000h. This bit will be set to '1' once accumulator underflows. Write '1' will clear this bit.
9	R/W	(REC_OVERUN) is recording overrun status bit. Active high. This bit will be set to '1' if recording is running & rec_req_ is active & data_rdy haven't come.
8	R/W	(PB_UNDERUN) is playback FIFO underrun status bit. Active high. This bit will be set to '1' if playback is running & FIFO is empty & f48 clock is coming.
7	R/W	(ST_IRQ) is Sample Timer IRQ bit. Active high. Bit[7] = ST_IRQ_En | ST_TARGET_REACHED
6	R/W	(ENVELOPE_IRQ) is Wave-table Envelope Engine IRQ bit. Active high. Bit[6] = | EINT[31:0]
5	R/W	(ADDRESS_IRQ) is Wave-table Address Engine IRQ bit. Active high. Bit[5] = (| AINT_A[31:0]) | (| AINT_B[31:0])
4	R/W	(OPL3_IRQ) is OPL3 timer IRQ bit. Active high. Bit[4] = timerirq & opltimer_ie
3	R/W	(MPU401_IRQ) is MPU401 IRQ bit. Active high. Bit[3] = mpu401irq (signal from Legacy Audio block)
2	R/W	(SB_IRQ) is sound blaster IRQ bit. Active high. Bit[2] = sbirq (signal from Legacy Audio block)
1	R/W	(REC_OVERUN_IRQ) is recording overrun IRQ bit. Active high. Bit[1] = OVERUN_IE & Bit[9].
0	R/W	(PB_UNDERUN_IRQ) is playback FIFO underrun IRQ bit. Active high. Bit[0] = UNDERUN_IE & Bit[8].

All other bits are reserved bits.

Register B4h STAR_B (START command and status register for Bank B)

Legacy Address:

Default Value: 0000h

Access: Read / Write

BIT	ACCESS	DESCRIPTION
31:0	R/W	This register and STOP_B are used as Bank B channel start/stop

		command register when they are written, and used as Bank B channel running/stopped status register when they are read. bit n is for channel n. Reading from this I/O port will return the running/stopped status of Bank B 32 voice channels. 0:Stopped. When bit n is read as '0', it means any operation of channel n, including address generation, sample data fetching, interpolation, and envelope calculation is stopped. And this channel has no contribution to the digital mixer. This bit will be reset from '1' to '0' in four cases. (1) when a '1' is written to the corresponding bit in register STOP_B. (2) when out of data, i.e. when sample loop disabled and CSO (Current Sample Offset) >= ESO (End Sample Offset). (3) when Ec (current envelope) drops down to -63.984375 dB. (4) when current envelope buffer is in delay-stop mode, and EDLY count down to '0'. 1:Running. When bit n is read as '1', it means channel n is working. This bit will be set from '0' to '1' only when a '1' is written to the corresponding bit in register START_B. Writing to this I/O port means issuing a start command to address engine and envelope engine in expected channel. 0:Ignore. A '0' written to bit n will not change the status of channel n. 1:Start. A '1' written to bit n will start channel n's address engine and envelope engine and also set the status bit n to '1'.

Register B8h STOP_B (Channel STOP command and status register for Bank B)

Legacy Address:

Default Value: 0000h

Access: Read / Write

BIT	ACCESS	DESCRIPTION
31:0	R/W	Reading from this I/O port will return the same value as from the last register START_B. Writing to this I/O port means issuing a stop command to

		address engine and envelope engine in expected channel. 0:Ignore. A '0' written to bit n will not change the status of channel n. 1:Stop. A '1' written to bit n will stop channel n's address engine and envelope engine, and also reset the corresponding status bit to '0'.

Register BCh CSPF_B(Bank B Current Sample Position Flag)

Legacy Address:

Default Value: 00000000h

Access: Read only

BIT	ACCESS	DESCRIPTION
31:0	RO	This register will show a flag which indicates the Bank B's current sample is in a range between ESO/2 to ESO or in a range before ESO/2 (ESO is offset from loop begin to loop end). And this flag will be used for sample data double buffering control. Bit n is for channel n. 0: Before ESO/2 1: From ESO/2 to ESO When channel n is stopped, bit n will be reset to '0'.

Register C0h SBBL & SBCL (Sound Blaster Base Block Length & Current Block Length)

Legacy Address:

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:0	R/W	SBBL(Bit 31-16) is sound blaster base block length SBCL(Bit 15-0) is current value of sound blaster block length counter If sound blaster DMA loop is enabled(SBCTRL[3]=1), every time when SBCL changed from 0 to FFFFh, a INT will be issued, the contents of SBCL is reloaded from SBBL, and DMA operation continues . If sound blaster DMA loop is not enabled(SBCTRL[3]=0), every time when SBCL changed from 0 to FFFFh, a INT will be issued, the contents of SBCL is reloaded from SBBL, and set LegacyCMD to 101(pause).

		SBCTRL bit 7 is used to determine the counter operation mode (byte count or word count). The counter is a count down counter.

Register C4h SBCTRL & SBE2R & SBDD (Sound Blaster Control)

Legacy Address:

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:24	R/W	is sound blaster DMA testing byte command data port(write only) Any time after Bit31-24 has ever been written, E2Status (source from wave engine) will be set high. E2Status will be cleared after the testing byte has been sent to the system location.
15:8	R/W	is sound blaster direct mode playback data port
7:0	R/W	is legacy sound blaster voice in/out control register
7	R/W	0:8 bit data format 1:16 bit data format
6	R/W	0:mono 1:stereo
5	R/W	0:unsigned data format 1:signed data format
4	R/W	0:playback 1:recording
3	R/W	sound blaster DMA loop enable control 0:loop disabled. 1:loop enabled.
2:0	R/W	LegacyCMD 000 stop : No any operation. No contribution to Digital Mixer 001 run : Normal operation. 010 silent_DMA : SBCL will count; CA, CBC won't count. No data fetching. No interpolation. No contribution to Digital Mixer 011 reserve 100 silent_SB : SBCL, CA & CBC will count as the same as run mode. No data fetching. No interpolation. No contribution to Digital Mixer 101 pause : SBCL, CA & CBC don't change. let SBALPHA unchanged, CACHE_HIT=1

		drive current LD (or LD_L, LD_R) to Digital Mixer 110 reserve 111 Direct_playback : SBCL, CA & CBC don't change. drive SBDD to Digital Mixer

Register C8h STimer (Playback Sample Timer)

Legacy Address:

Default Value: 00000000h

Access: Read only

BIT	ACCESS	DESCRIPTION
31:0	RO	Bit 31-0 (STimer) will show current state of the sample timer counter which will count up every f48k clock and will be reset when RST_Stimer bit being written. Active high.

Register CCh LFO_B And I2S_DELTA (Bank B Low Frequency Oscillator Control)

Legacy Address:

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:27	R/W	Reserved – Read Only 00000b
26:16	R/W	is used for Bank B LFO control
26	R/W	(LFO_E_B) is Bank B LFO enable bit. 0:disabled 1:enabled
25:24	R/W	(LFO_R_B) is clock rate select of Bank B LFO counter. 00:LFO counter clock rate is 48kHz 01:LFO counter clock rate is 48kHz/4 10:LFO counter clock rate is 48kHz/16 11:LFO counter clock rate is 48kHz/64
23:16	R/W	(LFO_INIT_B)is the initial value of the Bank B LFO counter which will count down to 0 then reload.
15:13	R/W	Reserved.
12:0	R/W	(I2S_DELTA) (Read only) This register returns the auto-detected DELTA of I2S input (f_{i2s}/f_{48k}).

Register D0h ST_TARGET (Sample Timer Target)

Legacy Address:

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:0	R/W	Bit 31-0 (ST_TARGET) is used to store a pre-set value. Once STIMER counter reaches that value, an IRQ called ST_IRQ will be issued if ST_IRQ_En = 1.

Register D8h AINT_B (Bank B address engine interrupt)

Legacy Address:

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:0	R/W	Any bits toggled from '0' to '1' will result in a IRQ. Reading from this I/O port will return the address INT status of Bank B's 32 channels. Bit n is for channel n. 0:No INT 1:INT This bit will be set in 2 cases: When CSO (current sample offset) >= ESO (end sample offset), and ENDLP_IE (end of loop INT enable bit in Global Control register) =1 and AINTEN_B bit n is set 1 for channel n. When CSO (current sample offset) >= ESO/2 (middle of ESO), and MIDLP_IE (middle of loop INT enable bit in Global Control register) =1 and AINTEN_B bit n is set 1 for channel n. Writing '1' to bit n of this register will reset this bit. 0:Ignore. A '0' written to bit n will not change the status of this bit. 1:reset A '1' written to bit n will reset this bit.

Register DCh AINTEN_B(Bank B Address Engine Interrupt Enable)

Legacy Address:

Default Value: 00000000h

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:0	R/W	This register will control address engine interrupt for each channel of Bank B. Bit n is for channel n.

		0:disable address engine interrupt for channel n 1:enable address engine interrupt for channel n

Register E0h E0h (CSO & ALPHA & FMS) (for Bank A & Bank B)

Legacy Address:

Default Value: XXXXXXXXh

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:16	R/W	(CSO) is the offset of current sample relative to loop begin sample.
15:4	R/W	(ALPHA) is sample interpolation coefficient, which stands for the linear interpolation ratio between current sample and the next one.
3:0	R/W	(FMS) is Frequency Modulation Step.

Register E4h (LBA) (for Bank A & Bank B)

Legacy Address:

Default Value: XXXXXXXXh

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31	R/W	(CPTR) is reserved for internal use of cache control
30:0	R/W	is the linear address of loop begin sample. It should be word aligned when sample type is 16-bit Mono or 8-bit Stereo; and should be double word aligned when sample type is 16-bit Stereo.

Register E8h (ESO & DELTA) (for Bank A & Bank B)

Legacy Address:

Default Value: XXXXXXXXh

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:16	R/W	(ESO) is the offset of loop end sample relative to loop begin sample.
15:0	R/W	(DELTA) is sample change step in format 4.12 (Four bits integer, 12 bits fraction), which stands for the frequency ratio: Fs/48KHz, while Fs is the sum of sample rate and pitch shifting rate

Register Ech (Bank A LFO_CTRL & LFO_CT & FMC & RVOL & CVOL) (Bank A Only)

Legacy Address:

Default Value: XXXXXXXXh

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:28	R/W	(SIN) Sine wave value.
27	R/W	(SIN_S) sign bit of sine wave. 0:positive 1:negative
26	R/W	(SIN_D) counter direction bit. 0:up 1:down
25:24	R/W	(LFO_R) LFO counter clock rate select bits. 00:48kHz 01:48kHz/4 10:48kHz/16 11:48kHz/64
23:16	R/W	(LFO_CT)LFO working counter.
15:14	R/W	(FMC) FM modulation control bits. 00:FMA = (FMS * SIN) >> 3 01:FMA = (FMS * SIN) >> 2 10:FMA = (FMS * SIN) >> 1 11:FMA = (FMS * SIN) >> 0
13:7	R/W	(RVOL)Reverb Send Linear Volume format: 1.6, 7Fh stands for 2x gain, 40h stands for no gain no attenuation, 00h stands for mute.
6:0	R/W	Chorus Send Linear Volume format: 1.6, 7Fh stands for 2x gain, 40h stands for no gain no attenuation, 00h stands for mute.

Register ECh (Bank B ATTRIBUTE & FMC & RVOL & CVOL) (Bank B Only)

Legacy Address:

Default Value: XXXXXXXXh

Access: Read/Write

BIT	ACCESS	DESCRIPTION

31:19	R/W	(ATTRIBUTE) Channel attribute
31:30	R/W	PB/REC Select 00:(Normal PB) Normal playback This is a normal playback channel in Bank B with Global Volume, Channel Volume, PAN, SRC, FM/AM features. In this case, bit[29:19] doesn't matter. 01:(Special PB) Special playback This channel can be one of several kinds of special playback channels. Bit[29:26] is used to select special playback type; bit[25:24] is used to select data flow from channel to FIFO; and bit[23:19] is used to enable/disable individual functions. 10:(REC) Recording to system memory This channel can be one of several kinds of recording channels. Bit[29:26] is used to select recording type; bit[25:24] is used to control how MONO sample is generated when recording; bit[23] is used to enable/disable SRC; bit[22:19] doesn't matter. 11:(REC_PB) Recording to system memory and playback to mixer This channel is a Recording channel which records sample data to system memory and playback to Main Mixer in the mean time. In this case, bit[29:26] is used to select recording type; bit[25:24] is used to control how MONO sample is generated when recording; and bit[23:19] is used to enable/disable individual functions.
29:26	R/W	Channel Type Select when Bit[31:30] is 00: (Normal PB) xxxx reserverd when Bit[31:30] = 01: (Special PB) 0000 playback to MODEM LINE1 Output FIFO 0001 playback to MODEM LINE2 Output FIFO 0010 playback to PCM L/R Output FIFO 0011 playback to HSET Output FIFO 0100 playback to I2S L/R Output Buffer 0101 playback to CENTER/LFE Output FIFO 0110 playback to SURR L/R Output FIFO 0111 playback to SPDIF L/R Output FIFO other reserved when Bit[31:30] = 1x: (REC or REC_PB) 0000 recording from MODEM LINE1 Input

		FIFO 0001 recording from MODEM LINE2 Input FIFO 0010 recording from PCM L/R Input FIFO 0011 recording from HSET Input FIFO 0100 recording from I2S L/R Input FIFO 0101 recording from MIC Input FIFO 0110 main mixer capture from PCM L/R Output FIFO 0111 main mixer capture from MMC L/R Output Buffer 1000 Reverb Send 1001 Chorus Send other reserved
25:24	R/W	Special Playback Channel to FIFO data flow select / Recording to MONO control When channel is in Special PB mode, this register is used to select input source of a stereo playback slot pairs such as PCM L/R, SURR L/R, CENTER/LFE, I2S L/R and SPDIF L/R. The input source of L/R can be from one channel or can be from two independent channels. When channel is in REC or REC_PB mode, this register is used to control how MONO sample is generated. when Bit[31:30] = 00 (Normal PB) xx never used when Bit[31:30] = 01 (Special PB) 00 Channel L/R to FIFO L/R In this case, channel is acting as a stereo channel, data flow is like Channel Left → FIFO Left Channel Right → FIFO Right 01 Channel L to FIFO L Data flow: Channel Left → FIFO Left 10 Channel R to FIFO R Data flow: Channel Right → FIFO Right 11 reserved when Bit[31:30] = 1x (REC or REC_PB) 00: left,

		01: right 10: (left+right+1)/2 11: reserved.
23	R/W	SRC Enable 0:disable 1:enable
22	R/W	FM and AM Enable 0:disbale 1:enable
21	R/W	PAN Enable 0:disable 1:enable
20	R/W	Channel Volume Enable 0:disable 1:enable
19	R/W	Global Volume Enable 0:disable 1:enable
18:16	R/W	Reserved
15:14	R/W	FM modulation control bits. 00:FMA = (FMS * SIN) >> 3 01:FMA = (FMS * SIN) >> 2 10:FMA = (FMS * SIN) >> 1 11:FMA = (FMS * SIN) >> 0
13:7	R/W	Reverb Send Linear Volume format: 1.6, 7Fh stands for 2x gain, 40h stands for no gain no attenuation, 00h stands for mute.
6:0	R/W	Chorus Send Linear Volume format: 1.6, 7Fh stands for 2x gain, 40h stands for no gain no attenuation, 00h stands for mute.

Register F0h (Bank A GVSEL & PAN & VOL & CTRL & Ec) (for Bank A only)

Legacy Address:

Default Value: XXXXXXXXh

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31	R/W	(GVSEL) is global volume select bit.

		0:select MUSICVOL 1:select WAVEVOL
30:24	R/W	(PAN) is Positioning attenuation control.
30	R/W	selects attenuated channel. 0: left, 1: right
29:24	R/W	is the attenuation value in format of 4.2. 3Fh stand for mute.
23:16	R/W	(VOL) is channel volume attenuation in format of 5.3. 00h stands for 0 dB attenuation, FFh stands for mute.
15:12	R/W	are control bits.
15	R/W	selects 8/16 bit sample data 0:8-bit data 1:16-bit data
14	R/W	selects mono/stereo sample data 0:mono 1:stereo
13	R/W	selects unsigned/signed sample data 0:unsigned 1:signed
12	R/W	is loop mode enable bit. 0:disable 1:enable
11:0	R/W	is current envelope in format of 6.6 (Six bits integer and six bits fraction). 00h stands for 0dB, FFh stands for -63.984375 dB.

Register F0h (Bank B GVSEL & PAN & VOL & CTRL & Bank A LFO_INIT)

Legacy Address:

Default Value: XXXXXXXXh

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31	R/W	(GVSEL) is global volume select bit. 0:select MUSICVOL 1:select WAVEVOL
30:24	R/W	(PAN) is Positioning attenuation control.
30	R/W	selects attenuated channel. 0: left, 1: right.
29:24	R/W	is the attenuation value in format of 4.2. 3Fh stand for mute
23:16	R/W	(LFO_INIT) is Bank A per channel LFO counter initial and reload value.

		Note: Any time when host write to RegECh[26:16] (LFO_CT), LFO_INIT should be written with the same value.
15:12	R/W	are control bits.
15	R/W	selects 8/16 bit sample data 0:8-bit data 1:16-bit data
14	R/W	selects mono/stereo sample data 0:mono 1:stereo
13	R/W	selects unsigned/signed sample data 0:unsigned 1:signed
12	R/W	is loop mode enable bit. 0:disable 1:enable
11:0	R/W	(VOL) is channel volume attenuation in format of 6.6. 000h stands for 0 dB attenuation, FFFh stands for mute.

Register F4h (EBUF1) (Bank A Only)

Legacy Address:

Default Value: XXXXXXXXh

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:30	R/W	(AMS_H) is Amplitude Modulation Step High part.
29:28	R/W	(EMOD) define operation mode. 00:DEC mode (ramp from 0dB to -64dB) In this mode, bits 7-0 of this register are used as ECNT which stores current state of a 8-bit counter; bits 15-8 of this register are used as EINIT which provides initial value of that 8-bit counter; bits 27-16 of this register are used as EAMT which is the absolute ramping amount with range from 0dB to 63 and 63/64 dB. Every 48KHz clock, ECNT decrease 1; every time when ECNT=00h, it reload EINIT, EAMT decrease 1, and Ec decrease 1; every time when EAMT=00h, envelope engine will toggle buffer flag in global register CEBC. 01:INC mode (ramp from -64dB to 0dB) In this mode, the layout of this register is completely the same as in DEC mode. Engine works in the same way except that the

		ramp direction is from -64dB to 0dB. 10:Delay mode In this mode, bits 27-26 are used to select sub-mode: 00:Delay_hold 01:Delay_start 10:Delay_stop 11:reserved 19-0 is used as EDLY which store the current state of a 20-bit delay counter, bits 25-20 are of no use. Every 48 KHZ clock, EDLY decrease 1. During all the time this buffer active, Ec keep unchanged. In Delay_hold sub-mode, when EDLY =00000h, engine will toggle current buffer flag in global register CEBC. In Delay_start sub-mode, when EDLY =00000h, engine will reset DLY flag register. In Delay_stop sub-mode, when EDLY =00000h, engine will reset start/stop flag register. 11:Still mode In this mode, Ec keep unchanged, buffer never toggle automatically. Only when CEBC is written, buffer may toggle.

Register F8h (EBUF2) (Bank A Only)

Legacy Address:

Default Value: XXXXXXXXh

Access: Read/Write

BIT	ACCESS	DESCRIPTION
31:0	R/W	EBUF2 is totally as the same as EBUF1except that bits 31-30 are AMS_L (Amplitude Modulation Step Low part).

9 ELECTRICAL CHARACTERISTICS